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Demonstration and characterisation of a non-inverting all-optical read/write regenerative memory

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ABSTRACT

An all-optical regenerative memory device using a single loop mirror and a semiconductor optical amplifier is experimentally demonstrated. This configuration has potential for a low power all-optical stable memory device with non-inverting characteristics where packets are stored by continuously injecting the regenerated data back into the loop.

1. Introduction

The capacity of optical communication links has grown significantly in recent years and it is possible to transmit data much faster than it is possible to process it. This is because of the relatively slow electronic technology often found in optical networks. Advances in all-optical processing techniques have been made including the development of components such as all-optical pre- and post-processing buffers [1–3]. There is still no all-optical alternative to electronic random access memory (RAM). So for solving conflicts, such as destination contention and pre-processing buffering, other methods need to be found.

The simplest way to store an optical signal is to propagate it through a medium, such as a length of fibre, where the storage period is defined by the propagation time. However, the length of the storage time is fixed to a (usually) small number of discrete values depending upon the position of predetermined taps (an example of this would be feed forward based packet switching [4]). An improvement over such a static situation can be obtained by incorporating switching in a series of delay lines so that the number of switches is logarithmically related to the number of possible delays. Another way to combat this issue would be to use a feedback architecture [5] where the output of a delay fibre is directed back into the input creating a re-circulating loop. The signal thus propagates around the loop in a pulse-preserving manner until the data is required. The limit with all pulse-preserving techniques is the capability to store data for extended periods of time where various physical effects, such as chromatic dispersion and attenuation, start to degrade the signal as they would with long transmission distances. This degradation can be avoided by periodically regenerating the stored data onto fresh pulses [1].

It has been previously demonstrated that a memory device can be created using an inverting shift register [6], this technique has the advantage that it utilises a single loop mirror as an optical switch, which copies the data stored onto fresh pulses after a period of time and is thus regenerative. However, when data is stored in the feedback loop, the data is inverted during each regeneration cycle, therefore the correct logical data can only be read for one cycle out of every two reducing access to the data. Previously non-inverting optical memory has been demonstrated [7] using an ultrafast non-linear interferometer configuration, however the operation of this device requires long lengths of birefringent fibre which would make hybrid integration difficult. This paper describes a new non-inverting optical memory device that has the advantage of being fully regenerative and provides potential for hybrid integration. A detailed characterisation of the operating regimes of the optical memory is presented.

2. Experiment

Regeneration is achieved using a terahertz optical asymmetric demultiplexer (TOAD) [8,9] which is based on a Sagnac loop mirror [9] with an SOA providing the non-linear element. Fig. 1 shows a

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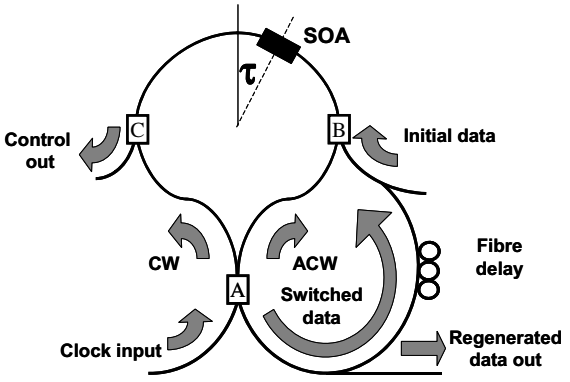

Fig. 1. Schematic diagram of the optical memory. The clock input is used to inject a continuous supply of fresh pulses to the optical switch. The Initial data input is used to load the memory.

schematic diagram of the full non-inverting optical memory consisting of a TOAD and fibre delay (feedback loop). Light injected at the clock input will enter the loop, coupler A, and separate into two signals propagating around the loop simultaneously in a clockwise (CW) and anticlockwise (ACW) direction until they re-enter the loop coupler. On re-entering the coupler the two pulses will re-combine, constructively in the case of perfect symmetry, back into a single pulse, which will exit through the port in which it originally entered. However, a π phase shift difference between the two-propagating signals re-entering the coupler will cause the light to exit through the opposite port to the clock input, labelled "switched clock" in Fig. 1. The phase shifts applied to the counter-propagating pulses depend on the population inversion of the SOA, as this determines the device's refractive index, as well as the position of the SOA in the loop. A control pulse injected into the loop, through coupler B, is used to create a time dependant inversion in the SOA. Since the propagating pulse signals arrive at different times they will see different phase shifts and hence the resultant output clock pulse will switch from the reflected clock input port to the transmitted data output port. The SOA offset from the centre of the loop determines the differential arrival times of the signal pulses and hence the switching window.

During the operation of the device a constant supply of clock pulses, provided at the system data rate, are available at the clock input, these pulses enter the loop and are all initially reflected back out of the clock input until data is required to be stored. To store data in the memory a data packet is injected into the control port, coupler B, just once. The data packet pulses act as control pulses and switch out the clock pulses into the feedback loop thereby mapping the data onto the new clock pulses, giving a regenerated version of the initial data. The switched out clock pulses then re-enter the TOAD but this time through the control port, as control pulses, where they switch out the next set of fresh clock pulses, which are then re-fed back into the feedback loop continuing the cycle. The data pulses are therefore regenerated and the pulses from the previous cycle are discarded at coupler C. It is possible to clear the stored data by blocking the feedback loop, preventing any switched clock pulses from entering the control port, and hence, breaking the cycle. Having successfully stored the data it is possible to read multiple copies of the data without affecting the data stored in the memory, as the data is continuously present at the data output port.

The experimental setup is shown in Fig. 2, a single fibre ring laser provided the source for both the clock and initial data pulses (10 Gb/s RZ pulses with a FWHM of 14 ps at a wavelength of 1550 nm). After the pulse source a 3 dB splitter separated the

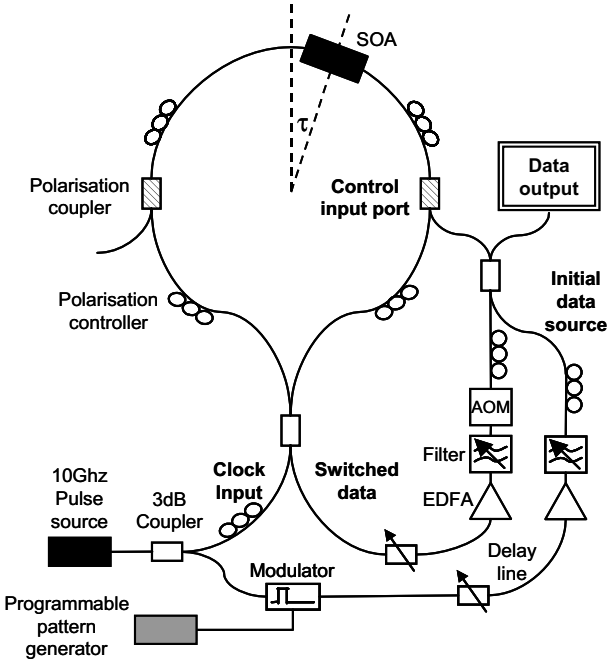

Fig. 2. Experimental setup, a fibre ring laser provides 10 GHz pulse streams for both the clock and the original data thus operating at the same wavelength. Before fresh data is stored the device is reset by disconnecting the feedback using an acousto-optical modulator (AOM). The data output is located at the end of the feedback just before the data re-enters the TOAD.

signal into two streams, one is used to provide the initial data and the other provided the clock pulses. The initial data packet was generated by modulating the pulse source using a lithium niobate ($LiNbO_3$) modulator. This packet was then amplified and filtered before being injected into the loop through the control port (this happens only once for a given packet). In the scheme demonstrated here, the clock and the data were at the same wavelength, it should be noted that the device would also work as a wavelength converter by having different clock and initial data wavelengths [10].

It is essential that control pulses be removed from the system, once they have switched out the clock pulses to become the next copy of the stored packet, as redundant pulses would cause the stored data to become corrupted. The control pulses were therefore removed with the polarization coupler C after they had transited through the SOA. The reset function was achieved by blocking the feedback using an acousto-optic modulator (AOM) for a time period matching the length of the loop. The length of the feedback loop (determined by the time taken for a switched out clock pulse to travel from the SOA around the feedback loop and back to the SOA as a control pulse) determines the maximum size of the packet that can be stored. Normally the stored packet size is slightly shorter than the maximum storage capacity, to allow a guard band between packets. The time taken for one circulation in the experiment described here was 5.5 μs and so the size of the stored packet must be smaller than this (55 kbs at 10 Gb/s).

Fig. 3a shows the original 44 kbs data packet or 4.4 μs of data consisting of five blocks of ones and four blocks of zeros (this simple data pattern was chosen as this could be easily seen on a real time oscilloscope). A space of 1 μs was included to enhance visual identification of the individual circulations. After the initial data packet enters the loop the packet is stored for 1 s, Fig. 3b. After one second the feedback loop is blocked which clears all data stored in the memory. Fig. 3c shows the last three blocks taken from Fig. 3b which can be compared with the initial input packet from Fig. 3a, we can see that the packet has been successfully

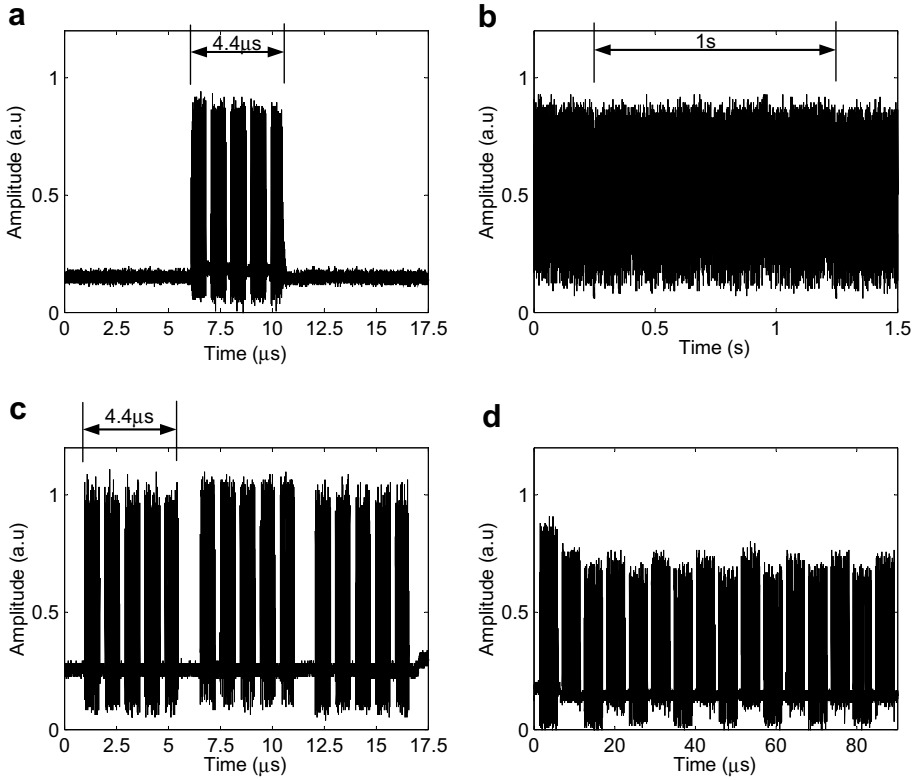

Fig. 3. Experimental traces showing the memory function (a) the initial data packet consisting of 44 kbs of data (equivalent to 4.4 μs), (b) data is stored for 1 s, (c) the final three blocks of stored data after 1 s of storage time (d) the initial 15 circulations of data storage demonstrating the self-levelling transient of the device.

stored. It can be seen in Fig. 3d that although the initial stored data is of relatively high amplitude, the pulse amplitudes evolve toward a stabilised level around which the amplitude of the blocks oscillate with a power variation between consecutive blocks of approximately 0.7 dB [11].

In order to provide a detailed characterisation of the device performance the initial data pattern was simplified to consist of only two blocks of ones separated by a short block of zeros whilst the total length remained at 44 kbs, Fig. 4. The results demonstrate the response of the device as a function of both peak power and data pulse timing for nine circulations (which is equivalent to 50 μs storage time).

First we study the performance of the memory as a function of the power of the initially injected data packet. Fig. 5a shows nine consecutive blocks stored in the memory for four different input power levels A = −30 dB m, B = −22 dB m, C = −12 dB m and D = −8 dB m. A more complete characterisation as a function of input power is shown in the intensity plot of Fig. 5b. Block 1 in Fig. 5a is the first circulation, switched out by the original data packet, followed by blocks 2–9. When the initial data packet power is too low, A, the initial switched out clock pulses, block 1, are not high enough in intensity for the device to recover the data to a stable level and so therefore the data is lost. As the data increases in power and a greater phase shift is created between the two-propagating pulses, B, the initial data power is lower than the stable level, however, the transmitted output is sufficient for the data to be stored and after every circulation the level of the ones continues to increase until the stable level is reached. When the initial data power is high enough to cause a full π phase shift, required to provide complete switching, the initial level is higher than the stable level, C. Therefore, the intensity of the levels reduces after every circulation, until the stable level is reached. During the operation of the device the stable level, defined by the gain in the feedback, is set to provide switching less than π to reduce the gain in the feedback and therefore suppressing propagating noise in the device. Any further increase of input power will generate a phase shift greater than π and so the intensity of the initial switched out block is reduced, D. In addition, the increase in the energy of the zeros (due a finite extinction level) will cause the zeros to turn into ones, corrupting the data. The actual value of the stable operating level changes with gain of the feedback path in a complex manner dependent on the switching curve of the TOAD and SOA gain. In this experiment the stable operating point corresponds to an average power of −16 dB m.

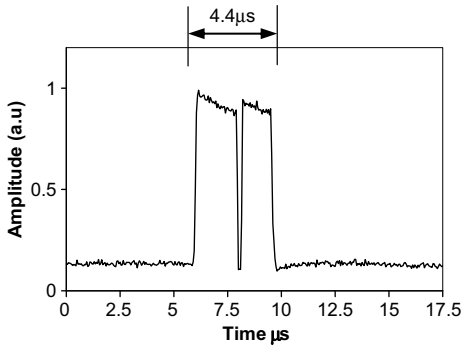

Fig. 4. Initial data pattern consisting of two blocks of 1 s separated by one block of 0 s. The total packet length used was 4.4 μs.

Fig. 5b shows the full sweep from A to D in an intensity graph from the point where no data is stored at the lower levels A up to the point where the amplitude of the initial data is too high and the definition of the zeros is lost D. Further increases in input power were limited by the risk of damage to the SOA, however we

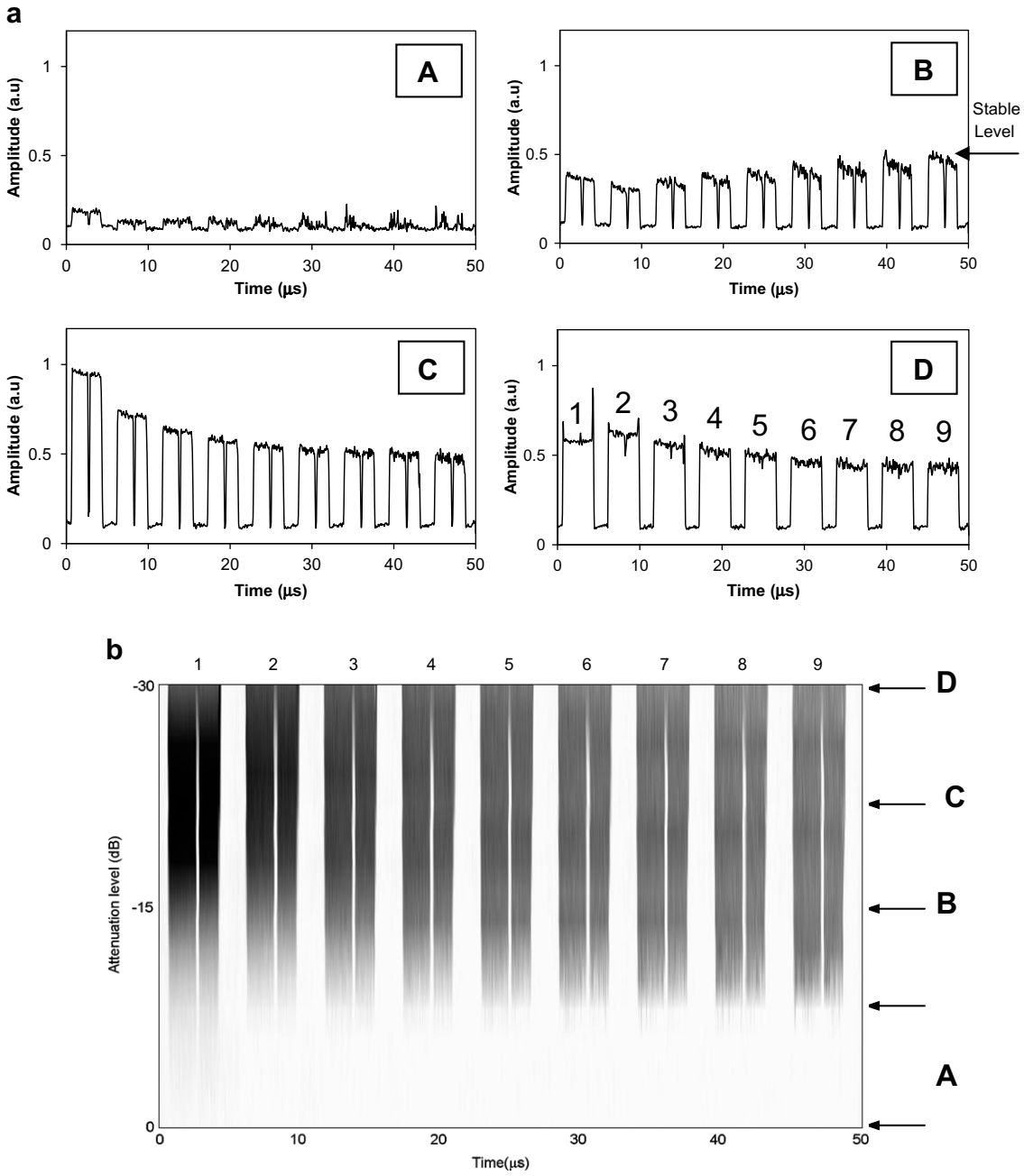

Fig. 5. Characterisation of the first nine circulations: (a) data stored recovering to a stabilised level, for changing input data powers and (b) the full range of varying initial data input powers, starting from where the initial data is too low and no data is stored, A. increasing to B and C where good contrast between the zero and one levels is maintained and finally the initial data packet power is high enough to cause the zeros to become ones thus corrupting the data, at D.

have found that the device will store data over a ~15 dB range in input power from ~−12.5 dB m to −27.5 dB m.

The arrival time of the control pulses at the SOA, with respect to the clock pulses, defines the switching efficiency of the TOAD, hence the optimum arrival time would allow for full switching to be achieved thereby producing maximum intensity at the data output. However, if a poor timing position is used then the TOAD would have a smaller transmission coefficient and thus the power at the data output would be low. Variations of initial data pulse timing with respect to the clock pulses are demonstrated in Fig. 6a and b. By changing the initial data timing, only, it can be demonstrated how tolerant the device is to phase wander (i.e. timing offset between the injected initial pulses and the clock stream) of the initial data input. We have already seen how the device reacts to a change in initial data power, by adjusting the timing of the initial data similar results should be obtained such that when the timing is in a poor position then there is not enough switched out power for the device to store the data. Alternatively, if the timing is moved to a more efficient position then the power of the initial switched out data will increase, therefore the data is recovered and through consecutive circulations the switched out power will increase until a stable level is reached. In Fig. 6 a delay time of 0 ps is defined as the position where the initial data timing is such that no pulses are switched out and hence the data cannot be recovered and therefore no data is stored. As the timing changes to 8 ps, Fig. 6a, the differential phase shift generated by the control pulses is increased therefore the intensity of the switched out clock pulses increases, allowing for the consecutive circulations to store the

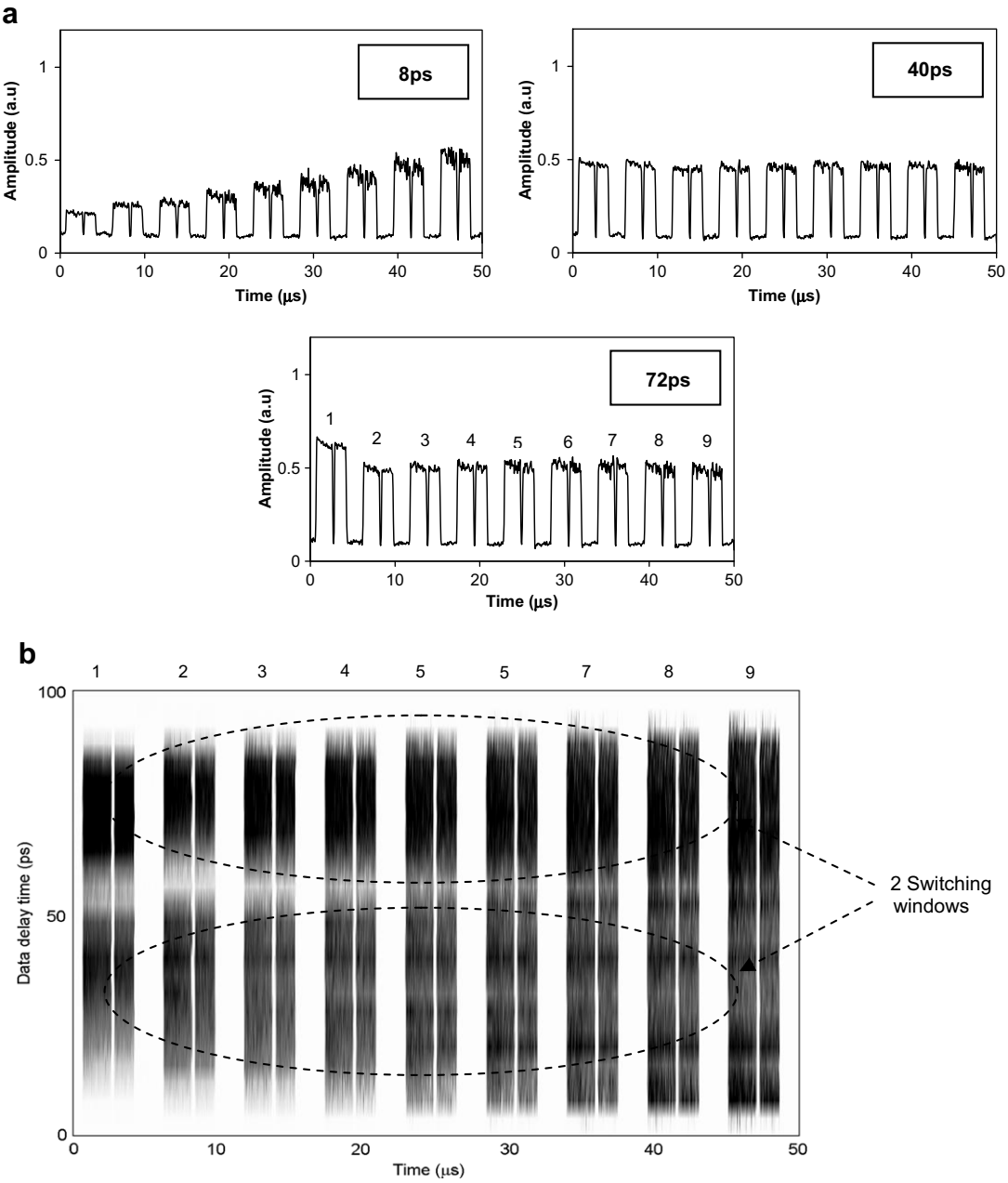

Fig. 6. Memory performance as a function of delay in the data. (a) variation in data pulse timings for the two optimum positions for each window of 40 ps and 72 ps and a less efficient operating position of 8 ps showing in all cases recovery to a stabilised level. (b) Full sweep of variation in input timings showing the two switching windows expected from a symmetrical SOA offset.

data. Note that there are two prominent switching windows over a delay variation of one bit intervals (100 ps). The location of the SOA, τ, is set to a 25 ps offset, which means that the counter and co-propagating pulses enter the SOA at equally spaced time intervals. In one window the counter-propagating pulses will see a saturated SOA and in the other window the co-propagating pulse will see the SOA in a saturated condition, hence two operating windows. By comparing the operating points, of 40 ps and 72 ps, it can be seen that the two windows are not identical, this is the result of the SOA being of finite length. With the initial data timing at its optimum point of 72 ps, defined by the amplitude of the output power, a maximum phase shift will be achieved and therefore the intensity of the output of the first circulation will be higher than the stable level, which is then reduced through consecutive circulations until the stable level is reached. It has been shown that the regenerative nature and the self-levelling ability provide for a large tolerance to input phase wander (timing with respect to the bit period) which in this case would be 40 ps in the initial data.

3. Conclusion

In conclusion we have demonstrated an all-optical memory device, which utilises only one SOA and a single optical loop mirror. The memory is non-inverting and consists of two inputs, a clock source and a port for loading the memory. The scheme has been experimentally demonstrated and is capable of storing a 4.4 kbit data packet for a period of 1 s (or 180,000 circulations of the loop). By varying the initial data input power and phase wander this has given an indication of the regenerative capabilities and the tolerance to noise. From the results it has been demonstrated that the

device is capable of storing data even when there is 40 ps of phase wander and a 15 dB variation in the optical peak power.

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