Self-consistent calculations of inversion-layer mobility in highly doped silicon-on-insulator metal–oxide–semiconductor field-effect transistors

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The inversion-layer mobility in future highly doped silicon-on-insulator (SOI) *n*-channel metal–oxide–semiconductor field-effect transistors (MOSFETs) has been examined for various SOI layer thicknesses (t_{SOI}) using self-consistent calculation. Not only phonon scattering but also surface roughness scattering and ionized impurity scattering have been taken into account. It has been found for SOI MOSFETs with a highly doped channel that, whenever t_{SOI} ($\gtrsim$2 nm) is reduced under the full-depletion condition, the inversion-layer mobility in SOI MOSFETs becomes higher than that in bulk MOSFETs. The increase in mobility with the reduction of t_{SOI} to about 10 nm is mainly caused by the suppression of surface roughness scattering. Independent of acceptor concentration (N_A), the mobility reaches its peak at t_{SOI} of about 3 nm and then decreases drastically with decreasing t_{SOI}. For SOI MOSFETs with N_A higher than $5\times10^{17}\,\mathrm{cm}^{-3}$, the mobility increases monotonously to the peak with decreasing t_{SOI} under the full-depletion condition due to the large suppression of ionized impurity scattering for the t_{SOI} range between 10 and 5 nm. These results are different from those in the previous works for SOI MOSFETs with low channel impurity concentration. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1378329]

I. INTRODUCTION

Recently, the gate lengths of silicon metal–oxide–semiconductor field-effect transistors (MOSFETs) approach sub-100 nm. Fully depleted silicon-on-insulator (SOI) MOSFETs are the most promising devices for future sub-100 nm MOSFETs because of the many advantages of these devices. Even if SOI substrates are used for MOSFETs with such ultrashort channels, the channel doping concentration has to become high. Therefore very thin SOI thicknesses are required for full depletion.

Recently, the phonon-limited inversion-layer electron mobility in ultrathin SOI MOSFETs has been studied using the self-consistent Schrödinger–Poisson calculation.[1,2] Shoji and Horiguchi[1] have reported that the mobility in SOI MOSFETs with a SOI layer thickness (t_{SOI}) more than 5 nm is almost equal to that in bulk MOSFETs, and that, as t_{SOI} decreases, the mobility increases to a maximum at t_{SOI} of about 3 nm and decreases abruptly. Takagi *et al.*[2] have shown that, as the t_{SOI} becomes smaller than 20 nm, the mobility decreases and then reaches its bottom at t_{SOI} of about 5 nm (for t_{SOI} below 5 nm, the dependence is the same as that in Ref. 1). However, in those works, low channel impurity concentration ($<10^{16}\,\mathrm{cm}^{-3}$) has been assumed, which is too low for future channel doping. Moreover, there may be mobility behaviors which cannot be seen from the calculation including only phonon scattering.

In this article the inversion-layer electron mobility in SOI *n*-channel MOSFETs with future highly doped channels is investigated for various t_{SOI}, using self-consistent calculations. Coulomb scattering by ionized impurities, which considerably affects the inversion layer mobility in bulk MOSFETs with a highly doped channel, and surface roughness scattering are also included in the mobility calculation. The effect of surface roughness scattering increases as the normal field becomes higher. It should be noted that the mobility of SOI MOSFETs is dependent on the SOI layer thickness because of the difference in effective normal electric field.

II. CALCULATION METHOD

The two-dimensional carrier distributions are evaluated by solving the coupled Schrödinger and Poisson equations self-consistently.[3,4] The Schrödinger equation is solved as an eigenvalue problem. The energy levels and wave functions of the subbands can be obtained by calculating the eigenvalues and eigenvectors of the discretized matrix. For these calculations, the bisection method and inverse iteration method are used. For the calculation of the discretized Poisson equation the incomplete Cholesky conjugate gradient (ICCG) method is employed. In this work the lowest 32 subbands are taken into account.

Not only intravalley and intervalley phonon scattering[5,6] but also surface roughness scattering and ionized impurity scattering are included in the calculation of the inversion layer mobility. For surface roughness scattering, the scattering rate model based on the exponential autocovariance function[7] is used. It was reported[7] that the mobility calculated with this model shows good agreement with experimental results. The scattering rate for surface roughness scattering is proportional to E_{eff}^2. Here E_{eff} is defined by

$$E_{\mathrm{eff}}=(q/\varepsilon_{\mathrm{Si}})(N_{\mathrm{depl}}+N_{\mathrm{inv}}/2), \tag{1}$$

where N_{depl} is the number of depletion charges per unit area and N_{inv} is the inversion electron density per unit area. As the

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inversion-layer thickness is restricted by the SOI thickness, the mobility may be affected by surface roughness scattering at the rear surface. However, that scattering is not taken into account because surface roughness scattering with normal field in the direction from silicon to oxide has not been modeled so far. Coulomb scattering by the ionized impurity significantly affects the mobility on the higher impurity substrate at lower normal field. The relaxation time for ionized impurity scattering from the ith subband with energy level E_i (wave vector $\mathbf{k}_i$) to the jth subband with energy level E_j (wave vector $\mathbf{k}_j$) is given by[8]

$$\frac{1}{\tau_{\mathrm{imp}}^{ij}(E)} = \frac{q^4 m_{di}}{8\pi\hbar^3 \varepsilon_{\mathrm{Si}}^2} \int_0^{2\pi} \frac{I_{ij}(Q(\theta))(1-\cos\theta)}{[Q(\theta)+PH_{ij}(Q(\theta))]^2} d\theta \cdot U(E-E_j), \tag{2}$$

$$P = q^2 N_{\mathrm{inv}}/(2\varepsilon_{\mathrm{Si}} k_{\mathrm{B}} T), \tag{3}$$

$$H_{ij}(Q) = \int_0^\infty \int_0^\infty \zeta_i(z_1)\zeta_i(z_2)\zeta_j(z_1)\zeta_j(z_2) \times \exp[-Q|z_1-z_2|]dz_1 dz_2, \tag{4}$$

$$I_{ij}(Q) = \int_0^\infty N_I(z_0)\left[\int_0^\infty \zeta_i(z)\zeta_j(z) \times \exp[-Q|z-z_0|]dz\right]^2 dz_0, \tag{5}$$

$$Q(\theta) = \sqrt{k_i^2 + k_j^2 - 2k_i k_j \cos\theta}, \tag{6}$$

where m_{di} is the density-of-states mass, $\zeta_i(z)$ is the wave function of the ith subband, $U(E)$ is the unit step function, and $N_I(z)$ is the ionized impurity concentration. The calculation of Eqs. (2)–(6) for all pairs of i and j needs a large amount of CPU time and is not practical. For MOSFETs with highly doped substrate almost all the inversion electrons exist in the lowest several subbands. Furthermore, the total intersubband scattering rate is considered to be much smaller than the total intrasubband scattering rate.[9] Therefore we include only five intrasubband transitions (three for the twofold valley and two for the fourfold valley).

All the simulations are carried out on (100) p-silicon at 300 K with zero back-gate bias. For simplicity the impurity concentrations in the SOI layer and in the substrate are assumed to be the same. The gate and buried oxide thicknesses are assumed to be 2 and 100 nm, respectively.

III. CALCULATED RESULTS AND DISCUSSION

Figure 1 shows the calculated inversion-layer mobility (μ) in bulk and SOI n-channel MOSFETs with various t_{SOI} as a function of effective normal field E_{eff}. The acceptor concentration N_A is $1\times10^{18}\,\mathrm{cm}^{-3}$. The mobility in bulk MOSFETs does not become very high due to the effect of ionized impurity and surface roughness scatterings (it deviates from the universal curve).[10–12] The mobility in SOI MOSFETs with larger t_{SOI} is also affected by ionized impurity scattering. As t_{SOI} increases, E_{eff} in SOI MOSFETs with the same N_{inv} becomes higher because of the increase in N_{depl} (E_{eff} in bulk MOSFETs is more than 0.5 MV/cm even if $N_{\mathrm{inv}}=0$). Therefore the inversion-layer mobility in highly doped SOI MOSFETs should not be compared at a constant E_{eff} for different t_{SOI}. We had better discuss comparing the mobility in a constant inversion state.

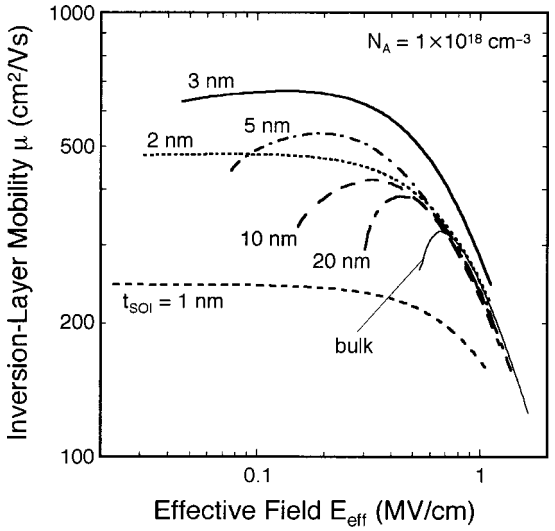

FIG. 1. Calculated inversion-layer mobility μ in bulk and SOI n-channel MOSFETs with various t_{SOI} as a function of effective normal field E_{eff}. $N_A=1\times10^{18}\,\mathrm{cm}^{-3}$.

Figure 2 shows the calculated N_{inv} dependence of the inversion-layer mobility in bulk and SOI n-channel MOSFETs with various t_{SOI}. Figure 3 shows the calculated t_{SOI} dependence of the inversion-layer mobility in SOI MOSFETs with N_{inv} of $2\times10^{12}\,\mathrm{cm}^{-2}$. The phonon-limited mobility, μ_{ph}, and the mobility including phonon and ionized impurity scatterings, $\mu_{\mathrm{ph+imp}}$, are also plotted. The differences between μ_{ph} and $\mu_{\mathrm{ph+imp}}$, and between $\mu_{\mathrm{ph+imp}}$ and μ, indicate the effects of ionized impurity scattering and of surface roughness scattering, respectively. As t_{SOI} decreases under the full-depletion condition (<38 nm), the depletion charge density in the SOI layer decreases, so that the effective nor-

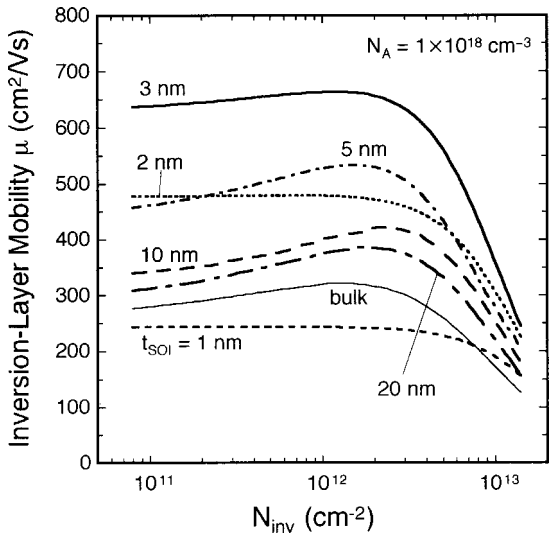

FIG. 2. Calculated inversion-layer mobility μ in bulk and SOI n-channel MOSFETs with various SOI layer thicknesses as a function of inversion electron density N_{inv}. $N_A=1\times10^{18}\,\mathrm{cm}^{-3}$.

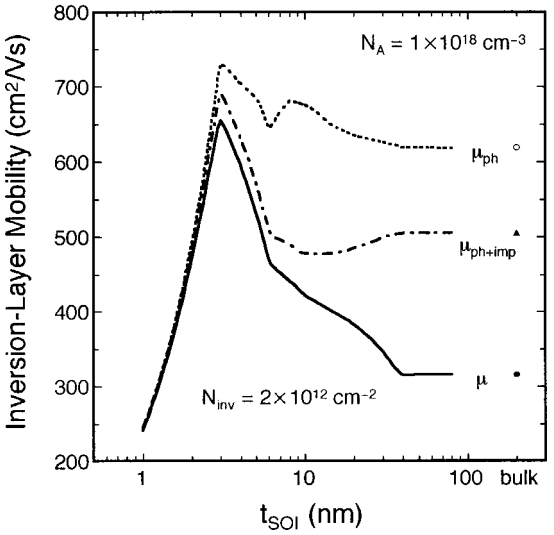

FIG. 3. Calculated inversion-layer mobility μ in SOI n-channel MOSFETs with N_A of $1\times10^{18}\,\mathrm{cm}^{-3}$ and N_{inv} of $2\times10^{12}\,\mathrm{cm}^{-2}$ as a function of SOI layer thickness t_{SOI}.

mal electric field at the surface becomes lower. Consequently, surface roughness scattering is more suppressed though ionized impurity scattering becomes stronger. However, the suppression in surface roughness scattering is much larger. Moreover, phonon scattering is also more suppressed, which is explained in the next paragraph. Thus the mobility increases with decreasing t_{SOI}.

Figure 4 shows the calculated t_{SOI} dependence of the average distance of inversion-layer electrons from the surface, that is to say, the quantum-mechanical inversion-layer thickness, z_{av}.[3] Here z_{av} is defined as

$$z_{\mathrm{av}}=\sum_i N_i z_i / N_{\mathrm{inv}}, \tag{7}$$

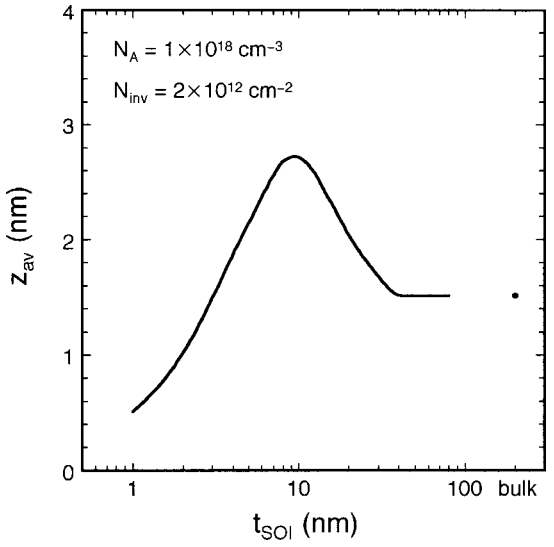

FIG. 4. Calculated average distance of inversion-layer electrons from the surface, z_{av}, as a function of SOI layer thickness t_{SOI}. z_{av} means the quantum-mechanical inversion-layer thickness. $N_A=1\times10^{18}\,\mathrm{cm}^{-3}$ and $N_{\mathrm{inv}}=2\times10^{12}\,\mathrm{cm}^{-2}$.

$$z_i=\int_0^\infty z\zeta_i(z)^2dz, \tag{8}$$

where N_i is the electron density per unit area in the ith subband. Because of the decrease in surface normal field, electrons around the surface shift in the direction of the bottom of the SOI layer (the occupation of electrons in subbands other than E_0 increases). Thus the inversion-layer thickness z_{av} increases. Generally, the scattering rates for both intravalley and intervalley phonon scatterings between the ith and jth subbands are proportional to the form factor, F_{ij},[1] which is defined by

$$F_{ij}=\int_0^\infty \zeta_i(z)^2\zeta_j(z)^2dz. \tag{9}$$

Moreover, it has been reported that F_{ij} is inversely proportional to the spatial extent of the wave functions.[1] The increase in the inversion-layer thickness leads to the increase in the spatial extent of the wave functions and the resultant decrease in F_{ij}. As a result, the phonon scattering rates decrease with decreasing t_{SOI}.

As shown in Fig. 4, the inversion-layer thickness starts to decrease at t_{SOI} of about 10 nm. This is because the extent of the wave function of electrons, particularly in subband $E_{0'}$, is restricted by very small t_{SOI}.[2] Since F_{ij} increases then, phonon scattering becomes stronger with decreasing t_{SOI} below 10 nm. Consequently, the phonon-limited mobility decreases, as shown in Fig. 3. However, ionized impurity scattering is more suppressed because of the decrease in the depletion layer thickness (ionized impurity scattering is caused by Coulomb potential arising from all charges located in the depletion layer). The decrease in the ionized impurity scattering rate exceeds the increase in the phonon scattering rate. Therefore the mobility still continues to increase. Not only when ionized impurity scattering is not taken into account but also when the channel impurity concentration is low or relatively low, the calculated mobility decreases in this t_{SOI} range. The latter case will be discussed later.

As t_{SOI} is reduced below 6 nm, since the energy level for subband $E_{0'}$ is raised due to the size effect of the ultrathin SOI layer, the difference in the energy level between the lowest two subbands becomes larger.[2] Consequently, the occupation of electrons in the lowest subband (E_0) increases and phonon scattering from subband E_0 to subband $E_{0'}$ and the other subbands is suppressed. In addition, ionized impurity scattering is further suppressed, as shown in Fig. 3. As a result, the inversion-layer mobility increases rapidly. At t_{SOI} below 3 nm, the effect of ionized impurity and surface roughness scatterings becomes very small, as shown in Fig. 3, and all the inversion electrons occupy only subband E_0. However, then the inversion-layer thickness is restricted by t_{SOI} since t_{SOI} is smaller than the inversion-layer thickness of bulk MOSFETs. In the case of such extremely thin t_{SOI}, the form factor is inversely proportional to t_{SOI}: $F_{ij}\propto 1/t_{\mathrm{SOI}}$.[1] As t_{SOI} decreases, the phonon scattering rates (proportional to the form factor) increase. Therefore the mobility drops drastically with decreasing t_{SOI}.

It has been reported that the mobility in SOI MOSFETs with t_{SOI} more than 5 nm is almost equal to that in bulk

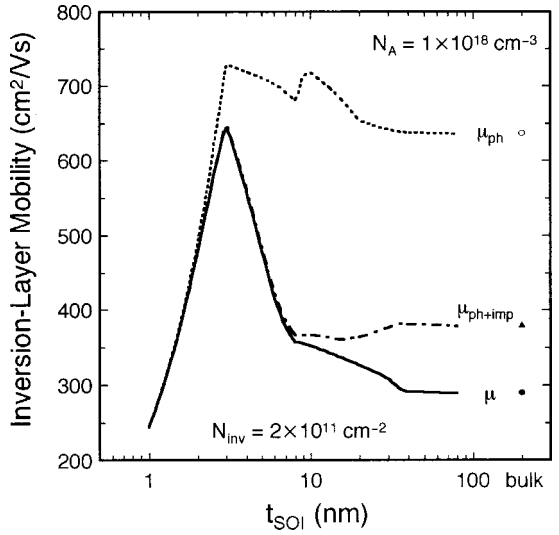

FIG. 5. Calculated inversion-layer mobility μ in SOI n-channel MOSFETs with N_A of $1\times10^{18}\,\mathrm{cm}^{-3}$ and N_{inv} of $2\times10^{11}\,\mathrm{cm}^{-2}$ as a function of SOI layer thickness t_{SOI}.

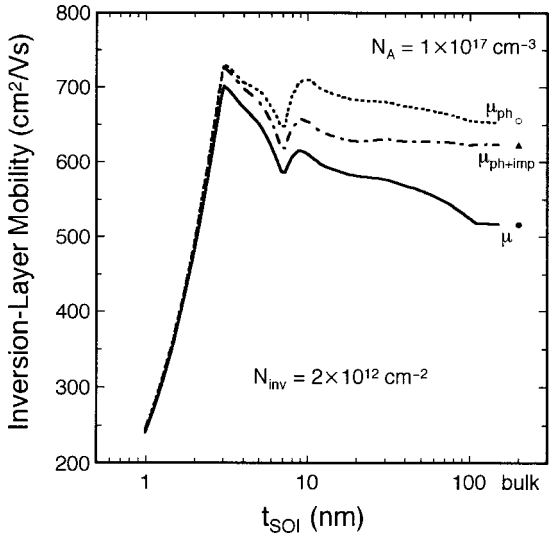

FIG. 6. Calculated inversion-layer mobility μ in SOI n-channel MOSFETs with N_A of $1\times10^{17}\,\mathrm{cm}^{-3}$ and N_{inv} of $2\times10^{12}\,\mathrm{cm}^{-2}$ as a function of SOI layer thickness t_{SOI}.

MOSFETs,[1] and that the mobility decreases with decreasing t_{SOI} less than 20 nm and then reaches its bottom at t_{SOI} of about 5 nm.[2] In those works the channel impurity concentration has been assumed to be too low for future channel doping. Those results are different from the above results for SOI MOSFETs with a highly doped channel.

The case for an inversion state other than the above is considered. Figure 5 shows the calculated t_{SOI} dependence of the inversion-layer mobility in SOI MOSFETs with N_{inv} of $2\times10^{11}\,\mathrm{cm}^{-2}$. Since N_{inv} is reduced, the effective normal field becomes low in all t_{SOI} ranges. Therefore the effect of ionized impurity scattering becomes much stronger than that of surface roughness scattering. Nevertheless, the mobility increases with decreasing t_{SOI} (>10 nm) due to the suppressions of phonon and surface roughness scatterings. Since the effect of ionized impurity scattering is extremely suppressed for t_{SOI} less than 10 nm, the mobility increases to the peak abruptly.

We discuss the case for SOI MOSFETs with relatively low channel impurity concentration. Figure 6 shows the calculated t_{SOI} dependence of the inversion-layer mobility in SOI MOSFETs with N_A of $1\times10^{17}\,\mathrm{cm}^{-3}$ and N_{inv} of $2\times10^{12}\,\mathrm{cm}^{-2}$. Then the t_{SOI} dependence of μ is qualitatively the same as that of the phonon-limited mobility μ_{ph}. The inversion-layer mobility starts to decrease at t_{SOI} of about 10 nm. This is because the effect of ionized impurity scattering is much smaller than that for N_A of $1\times10^{18}\,\mathrm{cm}^{-3}$.

Figure 7 shows the calculated t_{SOI} dependence of the inversion-layer mobility in SOI MOSFETs with N_{inv} of $2\times10^{12}\,\mathrm{cm}^{-2}$ for various channel impurity concentration N_A. Independent of N_A, the mobility reaches its peak at t_{SOI} of about 3 nm and then decreases drastically with decreasing t_{SOI}. For t_{SOI} of 2 nm or less, the value of the mobility does not depend on acceptor concentration. For SOI MOSFETs with N_A higher than $5\times10^{17}\,\mathrm{cm}^{-3}$, the mobility increases monotonously to the peak with decreasing t_{SOI} under the full-depletion condition because the enhancement of phonon scattering for a certain t_{SOI} range is compensated by the suppression of ionized impurity scattering. As N_A increases, the mobility increase to the peak becomes larger but the value of the peak decreases slowly.

VI. CONCLUSION

The inversion-layer mobility in SOI n-channel MOSFETs with a future highly doped channel on (100) surface have been investigated over a wide t_{SOI} range by solving the coupled Schrödinger and Poisson equations self-consistently. Not only intravalley and intervalley phonon scattering but also surface roughness and ionized impurity scatterings have been included in the calculation of the mobility. It has been found for SOI MOSFETs with a highly doped channel that,

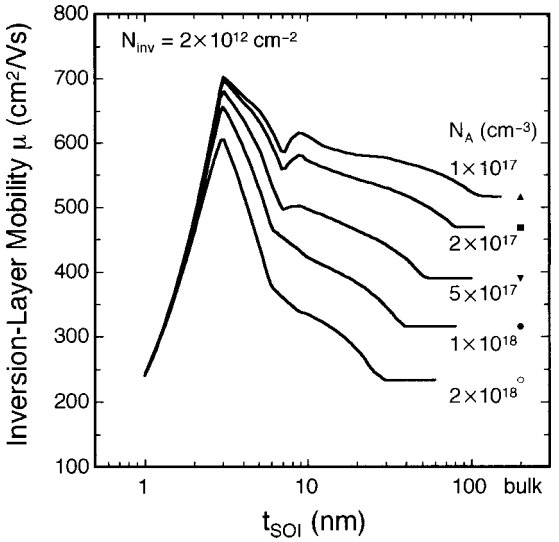

FIG. 7. Calculated inversion-layer mobility μ in SOI n-channel MOSFETs with various N_A as a function of SOI layer thickness t_{SOI}. $N_{\mathrm{inv}}=2\times10^{12}\,\mathrm{cm}^{-2}$.

whenever t_{SOI} ($\gtrsim$ 2 nm) is reduced under the full-depletion condition, the mobility in SOI MOSFETs becomes higher than that in bulk MOSFETs. Mainly because surface roughness scattering is much suppressed, the mobility increases with decreasing t_{SOI} from the depletion-layer thickness of bulk MOSFETs to about 10 nm. Independent of N_A, the mobility reaches a maximum at t_{SOI} of about 3 nm and decreases drastically with decreasing t_{SOI} below 3 nm. For SOI MOSFETs with N_A above $5\times10^{17}\,cm^{-3}$, the mobility increases monotonously to the peak with decreasing t_{SOI} under the full-depletion condition because the suppression of ionized impurity scattering exceeds the enhancement of phonon scattering in the t_{SOI} range from 10 to 5 nm. The t_{SOI} dependences of the mobility in this work are different from those in the previous works for SOI MOSFETs with low channel impurity concentration.

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