Electron transport in strained Si inversion layers grown on SiGe-on-insulator substrates

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We show by simulation that electron mobility and velocity overshoot are greater when strained inversion layers are grown on SiGe-On-insulator substrates (strained Si/SiGe-OI) than when unstrained silicon-on-insulator (SOI) devices are employed. In addition, mobility in these strained inversion layers is only slightly degraded compared with strained bulk Si/SiGe inversion layers, due to the phonon scattering increase produced by greater carrier confinement. Poisson and Schroedinger equations are self-consistently solved to evaluate the carrier distribution in this structure. A Monte Carlo simulator is used to solve the Boltzmann transport equation. Electron mobility in these devices is compared to that in SOI inversion layers and in bulk Si/SiGe inversion layers. The effect of the germanium mole fraction x, the strained-silicon layer thickness, T_{Si}, and the total width of semiconductor (Si+SiGe) slab sandwiched between the two oxide layers, T_w were carefully analyzed. We observed strong dependence of the electron mobility on T_{Si}, due to the increase in the phonon scattering rate as the silicon layer thickness is reduced, a consequence of the greater confinement of the carriers. This effect is less important as the germanium mole fraction, x, is reduced, and as the value of T_{Si} increases. For $T_{\mathrm{Si}}>20$ nm, mobility does not depend on T_{Si}, and maximum mobility values are obtained. © *2002 American Institute of Physics.*
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I. INTRODUCTION

One of the keys to the further improvement of complementary metal–oxide–semiconductors (CMOS) technology is the enhancement of carrier mobility in the device channel.[1] In recent years, much research activity has been focused on this task, considering the use of specific doping profiles, the growth of low doped epitaxial layers on high doped substrates,[2] or even the use of silicon-related materials instead of silicon. In relation to the latter proposal, a significant step was taken with the introduction of strained silicon to build the metal–oxide–semiconductor field-effect transistors (MOSFET) channel. Both theoretical and experimental studies have shown spectacular electron mobility enhancements when silicon is grown pseudomorphically on relaxed $Si_{1-x}Ge_x$.[3] The strain causes the six-fold degenerate valleys of the silicon conduction band minimum to split into two groups: two lowered valleys with the longitudinal effective mass axis perpendicular to the interface, and four raised valleys with the longitudinal mass axis parallel to the interface. This leads to a redistribution of the carriers between the different valleys. In the lowered valleys, which are more densely populated in the strained case, electrons show a smaller conduction effective mass (transverse mass) in transport parallel to the interface. In addition, the splitting between the valleys is enough to suppress the intervalley transitions of electrons from lower valleys to upper valleys, thus reducing the intervalley phonon scattering rate compared with that of unstrained silicon. The combination of a lower effective mass and reduced intervalley scattering gives rise to higher electron mobility. Moreover, the lower intervalley-scattering rates make energy-relaxation times higher, originating spectacular electron velocity overshoot, as shown elsewhere.[4] In spite of these important advantages, bulk strained $Si/Si_{1-x}Ge_x$ CMOS technology still suffers from some of the limitations of standard silicon CMOS technology for sub-0.1 μm applications.

Another candidate for sub-0.1 μm devices is the silicon-on-insulator (SOI) structure, due to the advantages of SOI devices compared to their conventional silicon counterparts, in particular with respect to radiation tolerance, lower parasitic capacitance, and short channel effects.[5–8] In contrast to strained-Si/SiGe technology, SOI technology is fully compatible with existing standard silicon fabrication facilities and, *a priori*, CMOS circuit designs could be translated to ultrathin SOI technology without much difficulty.[8]

However, although theoretical studies have predicted higher carrier mobility in ultrathin single-gate SOI samples compared to standard Si devices, this mobility increase (estimated in the best case at 10%) is obtained only for very low silicon layer thicknesses ($T_w<5$ nm) and for a high inversion charge concentration. In other cases, i.e., a greater silicon thicknesses, a mobility degradation is experimentally observed.[9–11]

One may wonder whether it would be possible to combine the two structures (strained silicon inversion layer and SOI inversion layers) to enjoy the advantages of each and at the same time, overcome the deficiencies they present separately. From the technology point of view, the answer is af-

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firmative. Very recent studies have reported the feasibility of fabricating SiGe-based SOI substrates by separation-by-implanted-oxygen techniques.[12,13] The fabrication of high-quality SiGe layers with a thickness of less than 10 nm on SiO_2 has also been demonstrated[12] (not without difficulty). Using these structures as a starting point, both *n*- and *p*-channel strained-SOI MOSFETs have been fabricated and successfully operated, showing high electron and hole mobilities with a germanium mole fraction as low as 0.1.[14–16] Other techniques have also shown the feasibility of fabricating Si/SiGe structures on insulator substrates, such as solid-phase epitaxy.[17–18]

Si/SiGe-on-insulator (SiGe-OI) structures provide a good control of short channel effects, have a lower parasitic capacitance and higher radiation tolerance and, moreover, present mobility values that are much higher than those found in conventional SOI MOSFETs. Nevertheless, to achieve these results and at the same time provide a low off-state leakage current, allow operation at low voltages and avoid the floating body effect, the Si/SiGe structure sandwiched between the two oxides must be thin enough ($T_w = T_{Si} + T_{SiGe} < 30$ nm,[8] where T_{Si} and T_{SiGe} are the thicknesses of the strained-Si layer and of the relaxed SiGe layer, respectively. On the other hand, in order to keep the strain, the silicon layer must be sufficiently thinner than the SiGe layer. Therefore, taking into account both conditions, ($T_w < 30$ nm and $T_{Si} < T_{SiGe}$), the strained-silicon layer thickness has to be reduced to a very low value ($T_{Si} < 10$ nm). With such small values of T_{Si}, the extension of the electrons in these structures is less than in bulk devices, which could lead to an increase in the phonon scattering rate, and therefore to a mobility decrease. This could partially counteract the mobility increase achieved by the strain effects (lighter conduction effective mass and reduced intervalley scattering). It is therefore interesting to study the relative importance of this effect, i.e., to determine whether this phonon scattering rate increase is produced, and in the affirmative case, for which T_{Si} values, if any, this phonon scattering rate counteracts the mobility increase produced by the strain.

To answer these questions, we studied the electron transport properties in these strained Si/SiGe-OI structures by the Monte Carlo method. The organization of this article is the following: Sec. II provides a brief description of the Monte Carlo simulator used. Section III describes how this simulator was used to study the behavior of the electron mobility in strained Si/SiGe-OI inversion layers as a function of the germanium mole fraction, *x*, the strain silicon thickness, T_{Si}, and the thickness of the potential well, T_w. We also analyzed another effect, which is even more important for very short channel devices than the reported mobility increase: this is the electron velocity overshoot, a function of the germanium mole fraction, Finally, the main conclusions are drawn.

II. MONTE CARLO SIMULATION

The feasibility of strained-Si/$Si_{1-x}Ge_x$ on insulator devices having been established, we investigated the behavior of charge carriers in these devices, to test whether they indeed take advantage of the combination of the two technologies. Figure 1 shows a cross section of the structure considered in this study. Taking a SiGe-OI substrate as a starting point, an undoped ultrathin strained-silicon layer is considered on the SiGe layer. To ensure that the silicon layer was strained, the thickness of the silicon layer was assumed to be, in all cases, less than that of the relaxed SiGe layer. An oxide 5 nm thick was deposited on the silicon layer, and on this, a polysilicon gate was assumed (Fig. 1). Electron quantization in the inversion layer was taken into account by self-consistently solving the Poisson and Schroedinger equations. A simple nonparabolic band model was assumed, taking $\alpha = 0.5\ \text{eV}^{-1}$. The effect of strain in the silicon layer is included only in the band structure as the valley splitting energy $\Delta E = 0.67x$ (x being the germanium mole fraction), assuming that the strain does not modify the shape of the valleys. Changes in nonparabolicity with strain are neglected as second-order effects. The effective mass of an electron is assumed to be the same as in unstrained silicon, as is usually done.[4,19]

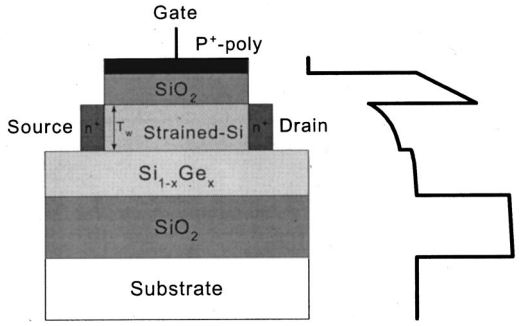

FIG. 1. Cross section of the strained-Si/SiGe-OI inversion layer under study. (Gate oxide thickness $T_{ox} = 5$ nm, buried oxide thickness $T_{box} = 80$ nm).

Once the electron distribution is known, the effect of a constant electric field, $E_{\parallel}$, applied parallel to the Si–SiO_2 interface is considered, solving the Boltzmann transport equation by the Monte Carlo method. $E_{\parallel}$ causes the electrons to drift along the channel where they are affected by different scattering mechanisms. It is known that scattering mechanisms related to the presence of nonideal semiconductor–insulator interfaces (mainly surface roughness and Coulomb scattering) limit the movement of electrons in the channel. The strained-Si and SiGe layers are intentionally left undoped. In addition, if the trap density at the interfaces with the SiO_2 is kept low, Coulomb scattering is very weak, and its effects cold be ignored. Therefore, only phonon scattering and surface-roughness scattering are taken into account in the simulation. We considered acoustic deformation potential scattering and intervalley phonon events. The coupling constants for the intervalley phonons and the acoustic deformation potential were the same as those used for unstrained silicon. The phonon-scattering rates for inversion layers were deduced by Price's formulation.[20] A detailed description of the method can be found elsewhere.[4,10] A new scattering model was used for surface-roughness scattering. The proximity of the upper and lower interfaces with the SiO_2 means that the usual Si/SiO_2 surface-roughness scattering model[21] for bulk silicon inversion layers is not useful: if the silicon layer is thin enough (thinner than 10 nm) the presence of the

buried interface plays a very important role, both by modifying the surface-roughness scattering rate due to the gate interface, and by itself providing a non-negligible scattering rate.[11] Moreover, the usual surface-roughness scattering model in bulk silicon inversion layers overestimates the effect of the surface-roughness scattering due to the gate interface as a consequence of the minimal thickness of the silicon layer. In order to account for this effect, an improved model was constructed, which made it possible to evaluate the surface-roughness scattering rate due to both the gate interface and to the buried interface.[11] Finally, we also assumed that the Si/SiGe interface is an ideal plane, i.e., there is no interface roughness scattering due to this interface. In addition, we have also ignored alloy scattering. Electrons are also scattered by the random nature of the SiGe alloy. This is a fundamental limitation that can not be removed (unless the alloy can be grown in an ordered form), but it is expected to have a weak effect in Si/SiGe system because only the tail of the electron distribution penetrates the SiGe layer.[22]

III. RESULTS AND DISCUSSION

Using the simulator just described, we studied the transport properties of electrons in strained-Si/SiGe inversion layers. The effect of the germanium mole fraction, x, the thickness of the strain silicon layer, T_{Si}, and the effect of the well width ($T_w = T_{Si} + T_{SiGe}$, T_{SiGe} being the thickness of the relaxed SiGe layer) are analyzed.

A. Effect of the germanium mole fraction (x)

As mentioned, the strain in the silicon layer produces two important effects, a lower conduction effective mass and a reduced intervalley scattering rate. These effects are more important as the strain becomes more important, that is, as the germanium mole fraction increases. To study the role played by x, we considered the strained-Si/SiGe-OI structure of Fig. 1 with $T_w = 10$ nm, $T_{Si} = T_{SiGe} = 5$ nm, and several values of the germanium mole fraction. Figure 2 shows the electron distribution in a strained-SOI inversion layer for different germanium mole fractions (symbols) and, for the sake of comparison, the electron distribution for unstrained SOI layers (with no SiGe layer) with $T_w = T_{Si} = 10$ nm (solid line—no symbols) and $T_w = T_{Si} = 5$ nm (dashed line—no symbols). Figure 2 also shows the electron distribution corresponding to a strained-Si/SiGe bulk inversion layer (no buried oxide) for $x = 0.3$ and $T_{Si} = 5$ nm (open symbols). Note that the discontinuity in the conduction band minimum at the Si/SiGe interface produces a greater confinement of electrons toward the Si/SiO_2 interface, which is more important as x increases. Note also that comparison of the curves corresponding to $x = 0.3$ for the Si/SiGe-OI case (bold squares) and for the bulk Si/SiGe case (open squares) reveals that the presence of the buried interface also leads to a greater confinement of the electrons in the former case. Greater carrier confinement always means less uncertainty in the location of the electrons in the direction perpendicular to the interface. In accordance with the uncertainty principle, there is a wider distribution of the momentum of the electron perpendicular to the interface. In other words, due to size quantization, the interface-directed momentum of the electron does not have a single value [as in three-dimensional (3D) electrons], but a distribution of likely values that expands as the silicon layer thickness is reduced. Taking into account the momentum conservation principle, there are more bulk phonons available that can assist in transitions between electron states, and therefore an increase in the phonon-scattering rate is expected. In consequence, for the same inversion-charge concentration, the phonon-scattering rate is greater in thinner films than in thicker ones (since the confinement is greater), and therefore a mobility reduction is expected. A more comprehensive explanation of the behavior of phonon-limited mobility in ultrathin SOI inversion layers with silicon layer thicknesses down to 10 nm can be found in Refs. 23 and 24 (and references therein). Numerically, this effect is reflected in the following form factor

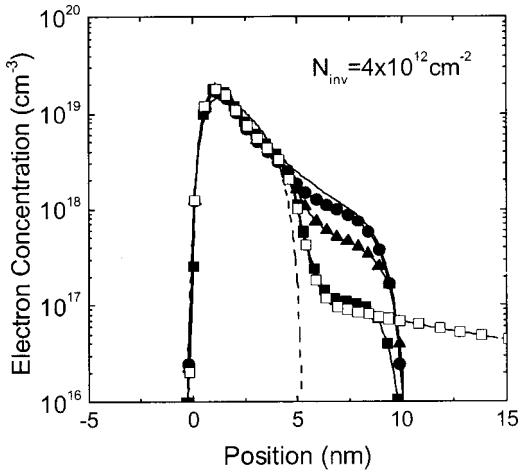

FIG. 2. Electron distribution for the simulated strained Si/SiGe-OI structure of Fig. 1 for different values of the germanium mole fraction, x: circles: $x = 0.1$; triangles: $x = 0.15$; squares: $x = 0.3$. ($T_{Si} = T_{SiGe} = 5$ nm). For the sake of comparison, electron distribution for unstrained SOI inversion layers is shown without symbols: dashed line: $T_{Si} = T_w = 5$ nm; solid line: $T_{Si} = T_w = 10$ nm. In open squares, electron distribution for a bulk Si/SiGe inversion layer with $T_{Si} = 5$ nm, and $x = 0.3$.

$$I_{\mu v} = \int_{-\infty}^{\infty} |\psi_\mu(z)|^2 |\psi_v(z)|^2 dz, \tag{1}$$

which multiplies the phonon scattering rates,[20] where $\psi_v(z)$ is the envelope of the electron wave function in the direction perpendicular to the interface in the vth subband. When confinement is greater (the overlap integral of envelope wave functions is also larger) the phonon scattering rate increases. Figure 3 shows the form factor for the ground subband in the same structure as in Fig. 2. Let us first consider the closed-symbol curves which correspond to strained-Si/SiGe-OI inversion layers with different values of x. As expected according to the aforementioned discussion, the greater the germanium mole fraction, the greater the form factor, and therefore the greater the phonon scattering rate. The least confinement in Fig. 2 corresponds to the SOI $T_w = 10$ nm curve. Accordingly, the lowest form factor curve (and therefore the lowest phonon scattering rate) corresponds, in Fig. 3, to this same device. In a similar way, the highest confinement corresponds to the SOI $T_w = 5$ nm curve, and the highest form factor curve and phonon scattering rate correspond

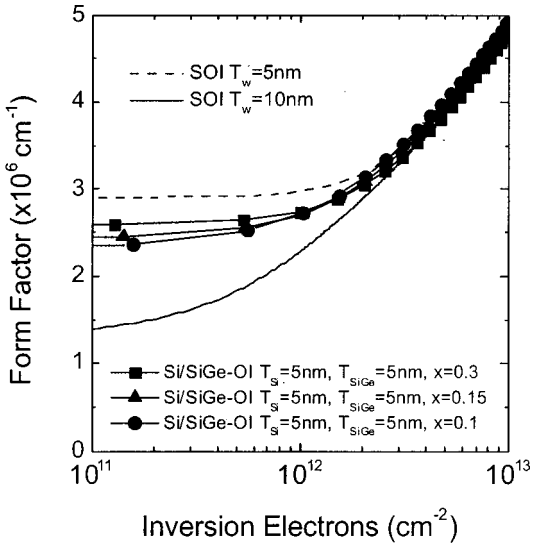

FIG. 3. (symbols) Form factor for the ground subband of strained-Si/SiGe-OI inversion layers with different values of the germanium mole fraction. (without symbols) Form factor for the ground subband of unstrained SOI inversion layers.

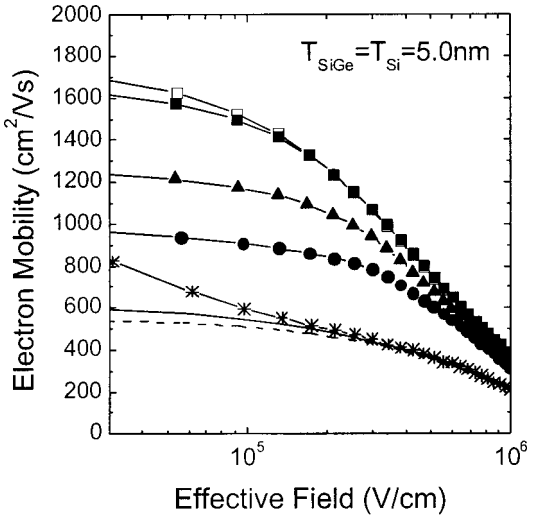

FIG. 5. Electron mobility curves versus the transverse effective field for the simulated curve of Fig. 1 at room temperature for different values of the germanium mole fraction, x: circles: $x=0.1$; triangles: $x=0.15$; squares: $x=0.3$ ($T_{Si}=T_{SiGe}=5$ nm). Phonon and surface roughness scattering are considered ($L_{sr}=1.5$ nm, $\Delta_{sr}=0.25$ nm). For the sake of comparison, mobility curves for unstrained SOI inversion layers are shown without symbols: dashed line: $T_{Si}=T_w=5$ nm; solid line: $T_{Si}=T_w=10$ nm. The mobility curve corresponding to a bulk strained-Si/SiGe inversion layer with $T_{Si}=5$ nm, and $x=0.3$ is represented by open squares. A mobility curve for a conventional bulk-silicon inversion layer is shown in asterisks.

in Fig. 3 to this device. In summary, either due to discontinuity of the conduction band minimum at the Si/SiGe interface or due to the semiconductor well width between the two oxides, an increase in the phonon scattering rate is expected as x increases, as T_{Si} decreases or as T_w decreases. According to this, one would expect the mobility curves to follow an inverse order to that shown in Fig. 3. However, we should not forget that the increase in the germanium mole fraction produces an increase in the strain in the Si layer and as a consequence, as discussed in the Introduction, a decrease in the conduction effective mass and a reduction in the intervalley scattering rate.[3,4] Figure 4 shows the evolution of the conduction effective mass with the electron concentration for the devices described in Fig. 2, where it can be seen that the greater the germanium mole fraction, the lower the conduction effective mass. If we turn now to the SOI curves (no symbols) we also observe a reduction in the conduction effective mass as T_w decreases. This effect is known as the subband modulation effect,[25] and has been extensively considered in Ref. 10. A comparison of the curves corresponding to the Si/SiGe-OI samples (symbols) and the SOI samples (no symbols) reveals that the subband modulation effect, that is, the reduction in the conduction effective mass, is more important in strained devices. Therefore, as x increases or T_w decreases, the conduction effective mass decreases and therefore the electron mobility should increase.

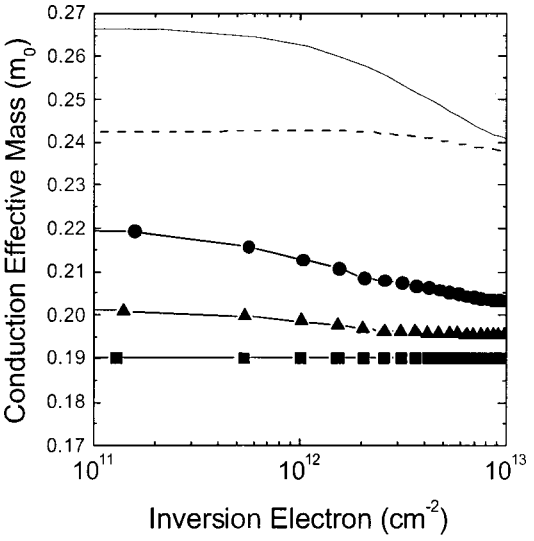

FIG. 4. (symbols) Conduction effective mass of electrons of strained-Si/SiGe-OI inversion layers with different values of the germanium mole fraction, x: circles: $x=0.1$; triangles: $x=0.15$; squares: $x=0.3$. ($T_{Si}=T_{SiGe}=5$ nm). For the sake of comparison, the conduction effective mass of electrons in unstrained SOI inversion layers is shown without symbols: dashed line: $T_{Si}=T_w=5$ nm; solid line: $T_{Si}=T_w=10$ nm.

In summary, we have two opposite trends concerning the mobility of electrons in strained Si/SiGe-OI inversion layers as the germanium mole fraction increases: (i) phonon scattering rate increase, and (ii) a conduction effective mass decrease. Therefore, the electron mobility behavior will depend on which of these factors is dominant. Figure 5 shows mobility curves versus the transverse effective field (as defined in Refs. 26 and 27), for the strained-Si/SiGe-OI inversion layers with different germanium mole fractions (symbols) described in Fig. 2. For the sake of comparison, the electron mobility curves for unstrained SOI layers with $T_w=T_{Si}=10$ nm (solid line—no symbols) and $T_w=T_{Si}=5$ nm (dashed line—no symbols) are shown. Figure 5 also shows a mobility curve corresponding to a strained-Si/SiGe bulk inversion layer (no buried oxide, for $x=0.3$ and $T_{Si}=5$ nm). Finally, Fig. 5 shows a mobility curve for a conventional bulk inversion layer (no buried oxide, and no SiGe) (asterisks).

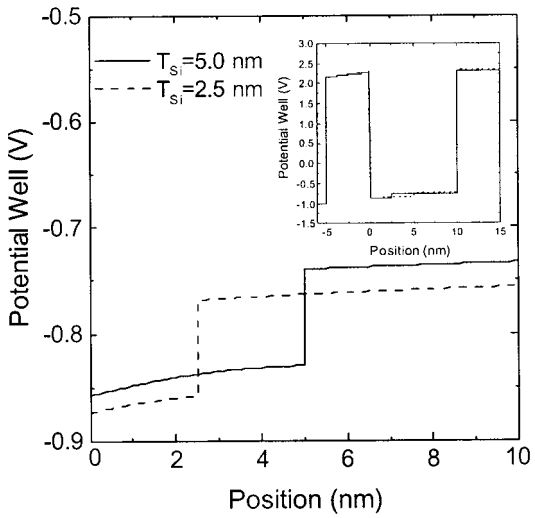

FIG. 6. Detail of the discontinuity of the conduction band minimum at the Si/SiGe interface of a strained-Si/SiGe-OI for two values of the strained silicon layer thickness ($T_w = 10$ nm, $x = 0.3$). (inset) Potential well for a strained-Si/SiGe-OI inversion layer for an inversion charge concentration of $N_{inv} = 5.3 \times 10^{11}$ cm^{-2}.

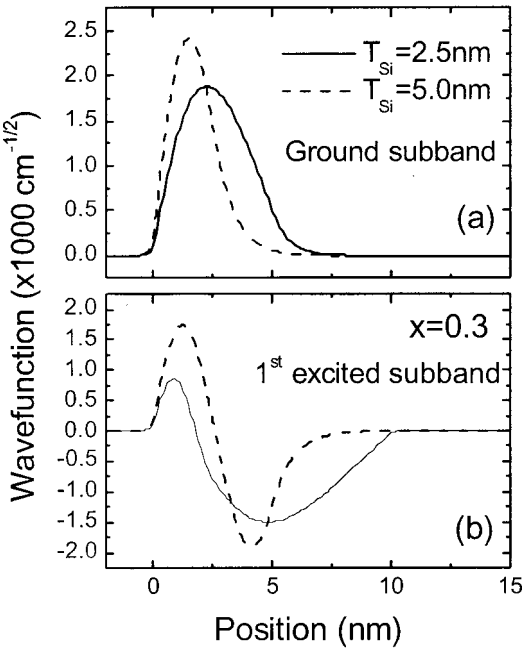

FIG. 7. (a) Wave functions for the ground subband and (b) for the first excited subband in a strained-Si/SiGe-OI inversion layer for two values of T_{Si}. ($T_w = 10$ nm, $x = 0.3$).

From the comparison of the different curves in Fig. 5, the following conclusions can be drawn:

(i) The first result obtained is an important increase in the electron mobility in strained-Si/SiGe-OI (bold symbols), as experimentally observed. Therefore, in these devices, the decrease in the conduction effective mass is dominant on the phonon scattering as the germanium mole fraction increases.

(ii) The opposite happens to unstrained SOI devices (no-symbol curves): the phonon scattering increase produced by the reduction in the potential well width is dominant on the subband modulation effect. In consequence, the mobility curve for SOI-$T_w = 5$ nm lies below the curve corresponding to the SOI-$T_w = 10$ nm device even when, as in Fig. 4, the latter device shows a higher conduction effective mass.

(iii) If we compare electron mobility for strained-SOI silicon inversion layers (solid squares) with the corresponding mobility for bulk strained Si-SiGe inversion layers (open squares), we observe a slight degradation at low transverse effective fields in the mobility curve corresponding to the strained Si-SiGeOI sample as a consequence of the greater confinement of electrons, which produces a slight increase in phonon scattering.

B. Effect of strained silicon layer thickness (T_{Si})

In the previous section we showed that the increase in the germanium mole fraction leads to a greater confinement of the electrons in strained-Si/SiGe-OI layers with the same values of T_{Si} and T_w. A similar effect is obtained if, for the same value of x, T_{Si} decreases. Figure 6 shows the potential well which confines the electrons in a strained-Si/SiGe-OI inversion layer for two values of silicon layer thickness ($T_{Si} = 2.5$ nm, dashed line and $T_{Si} = 5.0$ nm, solid line). the germanium mole fraction is considered to be $x = 0.3$, and the width of the potential well is considered to be $T_w = 10$ nm in both cases. The inset shows the whole potential well formed by the two oxide layers. Although T_w is the same in both structures, the discontinuity of the conduction band at the Si/SiGe interface leads to a greater confinement of the electrons. Figure 7 shows the wave function for the ground subband [Fig. 7(a)] and for the first excited subband [Fig. 7(b)]. As expected, the extension of wave functions is smaller as T_{Si} decreases. Figure 8 shows the electron distribution for both strained-Si/SiGe-OI inversion layers. The greater confinement of electrons in the sample with the thinner silicon layer leads to a greater phonon scattering rate as shown in Fig. 9. In the two samples considered, the germanium mole

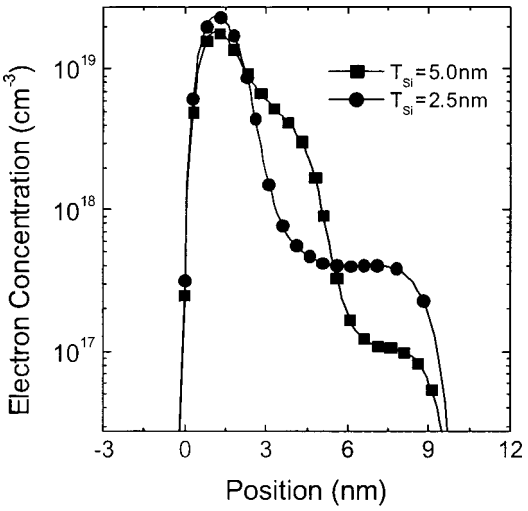

FIG. 8. Electron distribution for the simulated strained Si/SiGe-OI structure of Fig. 1 for different values of silicon layer thickness, T_{Si}. ($x = 0.3$, $T_w = 10$ nm, $N_{inv} = 4.0 \times 10^{12}$ cm^{-2}).

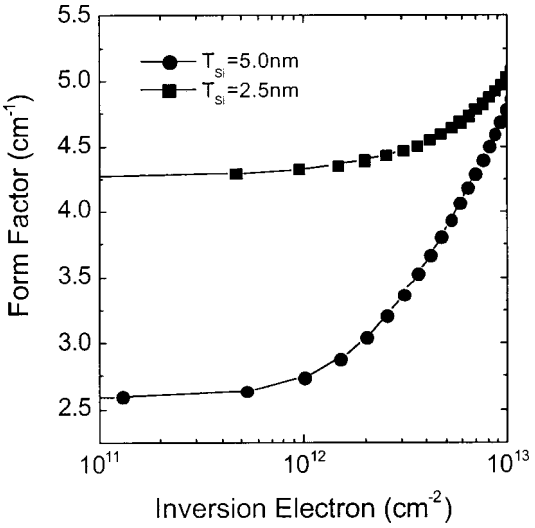

FIG. 9. Form factor for the ground subband of strained-Si/SiGe-OI inversion layers with different values of strained-Si layer thickness, T_{Si}. ($x=0.3$, $T_w=10$ nm).

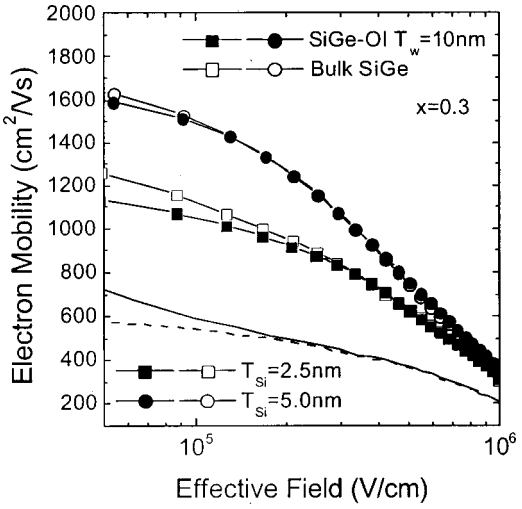

FIG. 11. (closed symbols) Electron mobility curves versus the transverse effective field for strained Si/SiGe-OI inversion layers at room temperature for different values of T_{Si}. ($T_w=T_{Si}+T_{SiGe}=10$ nm, $x=0.3$) (open symbols) Electron mobility curves versus the transverse effective field for strained Si/SiGe bulk inversion layers at room temperature for different values of T_{Si}. ($x=0.3$). (without symbols) Electron mobility curves versus the transverse effective field for conventional SOI inversion layers at room temperature for different values of $T_w=T_{Si}$.

fraction is set to $x=0.3$. In consequence, both silicon layers have the same strain, and fundamentally the same splitting between the two kinds of valleys of the silicon conduction band minimum. Therefore, the electrons basically have the same conduction effective mass regardless of T_{Si}, as shown in Fig. 10. The slight difference in the conduction effective mass which appears in Fig. 10 is a consequence of the greater confinement of the electrons. In summary, as the thickness of the strain silicon layer is reduced there is an important increase in the phonon scattering rate, while at the same time the conduction effective mass remains essentially the same, and therefore a degradation in electron mobility is expected. Figure 11 shows the mobility curves corresponding to the devices considered in Fig. 6 versus the transverse effective field. For the sake of comparison, we also show the mobility curves corresponding to strained-Si/SiGe bulk MOSFETs (no buried oxide) with the same T_{Si} (open symbols) and those corresponding to unstrained MOSFETs: the solid line represents an unstrained bulk MOSFET (conventional MOSFET), while the dashed line represents an unstrained SOI-MOSFET (conventional SOI MOSFET) with a silicon thickness of $T_w=T_{Si}=10$ nm.

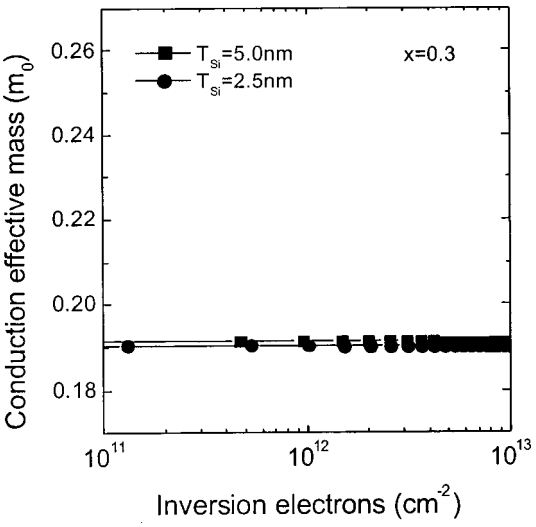

FIG. 10. Conduction effective mass of electrons in strained-Si/SiGe-OI inversion layers with different values of strained-Si layer thickness, T_{Si}. $x=0.3$. $T_w=10$ nm).

Figure 11 shows (as explained herein) that the electron mobility in the strained-si/SiGe-OI MOSFETs strongly depends on the T_{Si} value: the mobility curve corresponding to $T_{Si}=5$ nm (bold circles) is much higher than that corresponding to $T_{Si}=2.5$ nm (bold squares). As observed, this behavior is not exclusive to the Si/SiGe-OI structure (bold symbols), but also appears in the bulk Si/SiGe structures (open symbols). Once again, we observe that the mobility curves corresponding to strained-Si/SiGeOI MOSFETs (bold symbols) are slightly lower than those corresponding to strained-Si/SiGe bulk MOSFETs (open symbols), especially at low transverse effective fields. This is due to the greater phonon scattering rate in the SiGe-OI case, as a consequence of the greater confinement of the carriers in the well formed by the two oxide layers (T_w).[7,10] We also studied the effect of T_{Si}, as the germanium mole fraction is reduced. Figure 12 shows the same mobility curves as in Fig. 11 but in this case a germanium mole fraction of $x=0.1$ is assumed. Here, the dependence of the mobility on T_{Si} is lower for smaller germanium mole fractions. The reason for this is that the discontinuity of the conduction band is smaller, and therefore, the confinement of the carriers depends to a lesser extent on T_{Si} (the strain silicon layer thickness). Finally, we sought to determine the minimum value of T_{Si}, T_{Si}^*, on which the mobility in a strained-Si/SiGe-OI inversion layer depends, i.e., when the same mobility curves are obtained for $T_{Si} > T_{Si}^*$. To do this, we considered a bulk strained-Si/SiGe inversion layer and different values of T_{Si}. The results are shown in Fig. 13. As observed, for $T_{Si}>20$ nm, the mobility

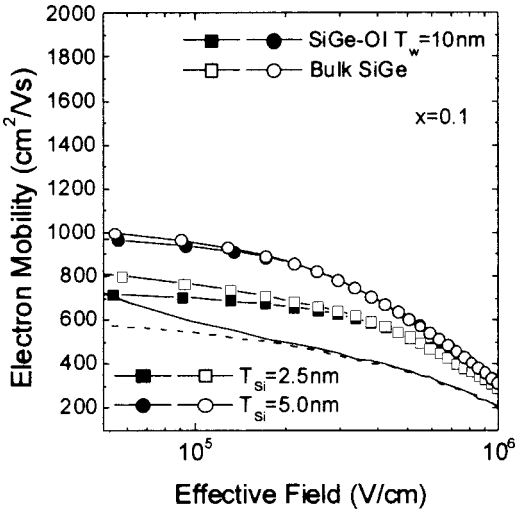

FIG. 12. (closed symbols) Electron mobility curves versus the transverse effective field for strained Si/SiGe-OI inversion layers at room temperature for different values of T_{Si}. ($T_w = T_{Si} + T_{SiGe} = 10$ nm, $x = 0.1$). (open symbols) Electron mobility curves versus the transverse effective field for strained Si/SiGe bulk inversion layers at room temperature for different values of T_{Si}. ($x = 0.1$) (without symbols) Electron mobility curves versus the transverse effective field for conventional SOI inversion layers at room temperature for different values of $T_w = T_{Si}$.

curves coincide. Thus, we estimate that the maximum mobility values are obtained for $T_{Si} > 20$ nm. For lower values, a degradation in the mobility curve is observed as a consequence of the increase in the phonon scattering rate, due to the greater confinement of the carriers caused by the discontinuity of the conduction band minimum at the Si/SiGe interface.

C. Effect of potential well width (T_w)

Figure 14 shows electron mobility curves versus the effective field for strained-Si/SiGe-OI inversion layers with different values of the potential well width, i.e., the width of the semiconductor layer sandwiched between the two oxides ($T_w = T_{Si} + T_{SiGe}$). The germanium mole fraction was considered to be $x = 0.3$ and the strained silicon layer thickness was set at $T_{Si} = 2.5$ nm. The thickness of the SiGe was modified from a minimal value $T_{SiGe} = 2.5$ nm to $T_{SiGe} = \infty$ (i.e., a bulk strained Si/SiGe structure). As can be observed in Fig. 14, the smaller T_w, the lower the mobility. This behavior is analogous to that experimentally observed in SOI inversion layers as the silicon thickness is reduced, and which can be explained in terms of an increase in the phonon scattering rate as the confinement of electrons increases when T_w is reduced (for a detailed discussion see Ref. 10). However, this mobility decrease is much less than that observed when T_w, T_{Si} is reduced (compare Figs. 11 and 14). Note that although the confinement of carriers in these structures depends on two variables, T_w and T_{Si}, it is the silicon layer thickness, T_{Si}, that is the principal factor. Therefore, a modification in T_{Si} has much more importance on electron mobility than a modification of T_w (with T_{Si}).

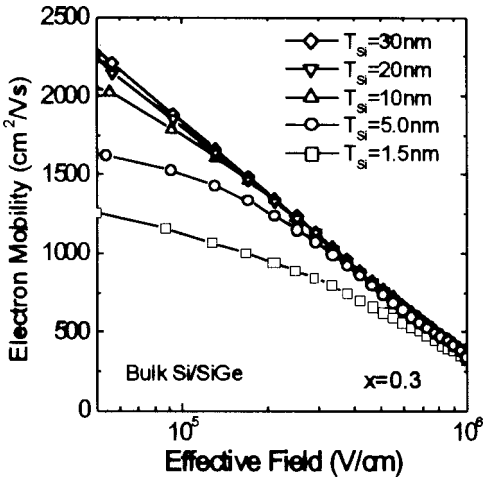

FIG. 13. Electron mobility curves versus the transverse effective field for strained Si/SiGe bulk inversion layers at room temperature for different values of T_{Si}. ($x = 0.3$).

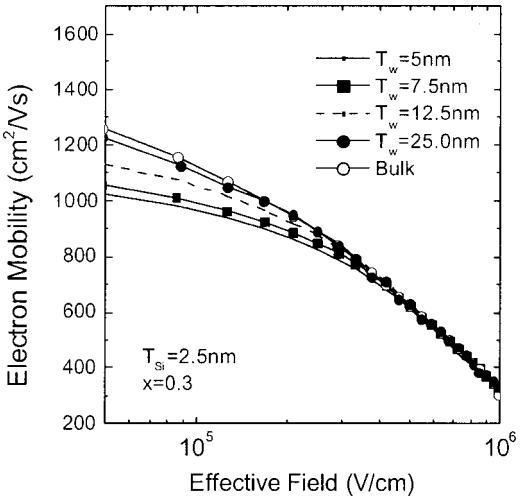

FIG. 14. Electron mobility curves versus the transverse effective field for strained Si/SiGe-OI inversion layers at room temperature for different values of T_w. ($x = 0.3$, $T_{Si} = 2.5$ nm).

D. Electron velocity overshoot

We have analyzed another effect which is even more important for very short channel devices than the reported mobility increase, namely the electron velocity overshoot.[28] We studied velocity-overshoot effects by applying a sudden high longitudinal electric field, E_2, to a steady-state electron distribution achieved under the influence of a low electric field E_1 (see insets of Fig. 15). The time evolution of the electron velocity is shown in Fig. 15 for different Ge mole fractions, and for two different values of E_2. It can be seen that the electron velocity quickly reaches and exceeds the new steady-state value. It then falls to approach this value (which is greater than the saturation velocity). Figure 15 shows that the time, t_s, the average electron velocity takes to reach the new steady-state value is greater as the germanium mole fraction increases ($t_s = 0.3$ ps$\Rightarrow x = 0.3$, $t_s = 0.2$ ps$\Rightarrow x = 0.15$, $t_s = 0.14$ ps$\Rightarrow x = 0.1$). In addition, the velocity peak reached by the electrons also increases as the Ge mole fraction increases.

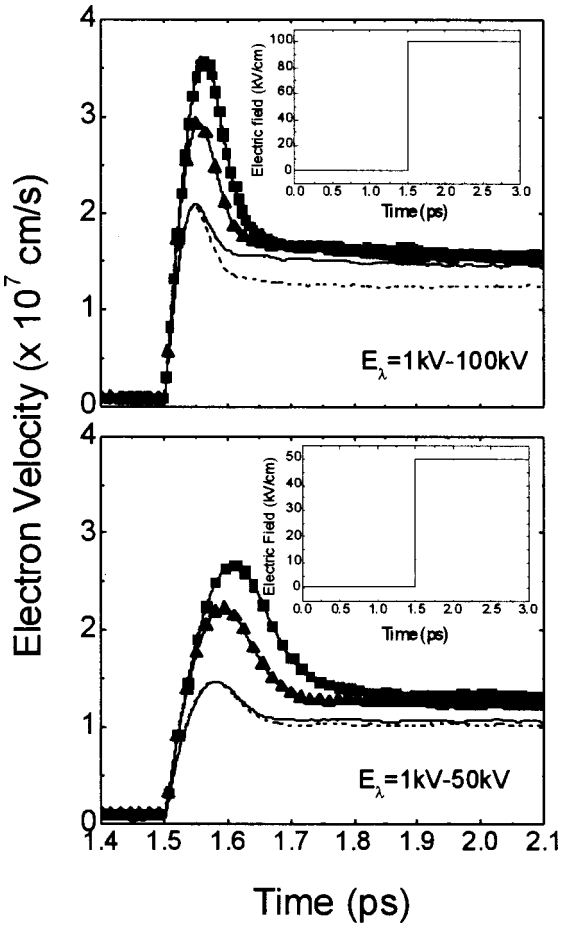

FIG. 15. Electron velocity overshoot transient resulting from the sudden application of a drift electric field E_2 for different values of the germanium mole fraction (triangles: $x=0.15$; squares: $x=0.3$) in strained Si/SiGe-OI inversion layers ($T_{Si}=5$ nm, $T_w=10$ nm, $x=0.3$) and in an unstrained SOI inversion layer (dashed line: $T_{Si}=5$ nm; solid line: $T_{Si}=10$ nm).

IV. CONCLUSIONS

We used a Monte Carlo simulator to study the electron transport properties of electrons in strained-Si/SiGe-OI inversion layers. The electron quantization was considered by self-consistently solving the Poisson and Schroedinger equations. Phonon and surface roughness scattering were taken into account. The behavior of the electron mobility with the germanium mole fraction, strained silicon layer thickness, and potential well width are analyzed and theoretically justified. The Monte Carlo simulator was also used to study the electron velocity overshoot.

In summary, we show that both the electron mobility and velocity overshoot effects are greatly improved in strained Si/SiGe-OI devices, in comparison with unstrained SOI devices. In addition, when we put these strained-SOI devices side by side with strained silicon devices, the degradation in the electron mobility due to the electron confinement caused by the presence of the buried oxide is weak (about 10%) if $T_w>10$ nm. Therefore, we conclude that strained-Si/SiGe OI inversion layers efficiently combine the improved mobility and velocity overshoot of strained-Si/SiGe devices with the advantages offered by SOI device. However, we also show the important role played by the strained silicon layer thickness on electron mobility. We observed that electron mobility in strained-Si/SiGe-OI inversion layers is strongly dependent on T_{Si}, due to the increase in the phonon scattering rate as the silicon layer thickness is reduced, a consequence of the greater confinement of the carriers. This effect is less important as the germanium mole fraction, x, is reduced, and as the value of T_{Si} increases. For $T_{Si}>20$ nm, mobility does not depend on T_{Si}, and the maximum mobility values are obtained.

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