# Nanoscale capacitors based on metal-insulator-carbon nanotube-metal structures

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We report the fabrication process and the electrical characteristics of a nanocapacitor structure using metal-insulator-carbon nanotube-metal layers. The structure shows high capacitance and the possibility of ultrahigh integration density due to the unique nanotube structure. Nanoscale and high-aspect-ratio patterns are achieved by electron beam lithography for the fabrication of these vertical nanostructures. This structure can be substituted for capacitors based on the silicon pillar structure in dynamic random access memory or as a nanoscale capacitor for various nanoelectronic devices. © *2005 American Institute of Physics*. [DOI: 10.1063/1.2149982]

Higher capacitance structures, than is possible with conventional silicon processing, are required to maintain the growth in integration density of electronic devices and circuits. Although many high-*k* dielectric materials have been investigated as a basis for a solution, their use in Si technology is complicated by the need for a complex bottom electrode structure or low reliability.[1,2] For dynamic random access memory (DRAM), the silicon pillar structure has been used instead of high-*k* dielectric materials to achieve high capacitance structures as the cell size is reduced. However, the process conditions required for lithography and etching become severe and more complicated as the integration density increases beyond the present levels.[3,4] A mixed approach, where structures using nanowires or nanotubes are grown,[5–7] rather than patterned and etched, can be a solution. The combination of a multiwall carbon nanotube (MWCNT) growth process with traditional silicon processing can be a viable route to achieving the requirement of high capacitance with nanoscale structures. Single MWCNTs can be grown vertically by direct current plasma enhanced chemical deposition (dc-PECVD) in selected positions, using a submicrometer patterned catalyst.[8] From this process, nanopillar structures with a high aspect ratio, having a diameter below 100 nm and several micrometers in height, can be fabricated in a relatively straightforward manner without the use of complex etch processes. However, a high vertical aspect ratio structure can be a problem for lithography steps which follow the pillar/tube making process. Spin coating is a well known technique for resist coating of a substrate, but it has a poor step coverage properties. In present DRAM processing, the resist layer is thicker than the silicon pillar height to solve this problem. However, this results in thick resist layers that limits the minimum feature size achievable using lithography. Therefore, the development of a lithographic process, compatible with a high aspect ratio, is essential when using bottom up grown vertical structures in integrated circuit (IC) applications.

Here, we report on the electrical characteristics and the fabrication process of metal-insulator-carbon nanotube-metal (MICNM) layer based vertically grown MWCNTs. In addition, we show a technique, based on electron beam (e-beam) lithography using thick resist for obtaining high aspect ratio vertical nanostructures. The approach presented here can overcome some of the previously mentioned challenges and allows the possibility of reducing capacitor size in ICs. This structure can be substituted for silicon pillars in DRAMs as well as being used as a general nanoscale capacitor.

Figure 1 shows the fabrication process of the MICNM structure. A Nb thin film was deposited by sputtering on the substrate as the bottom electrode, and then, a Ni catalyst layer was formed at selected positions by electron beam lithography together with lift-off technique. A dc-PECVD process was used for vertical MWCNT growth. A detailed description of MWCNT growth through this process can be found elsewhere.[8] The insulator layer, a $Si_3N_4$ layer was deposited by PECVD using a $SiH_4$ and $NH_3$ gas mixture. The dielectric constant of the film is 5.54. An Al layer was formed as top electrode by angular thermal evaporation (from $-45°$ to $45°$). The area of the top electrode was $220\ \mu m \times 320\ \mu m$.

Scanning electron microscopy (SEM) images of the MICNM structure are shown in Fig 2. A single MWCNT was grown vertically on each patterned catalyst dot of 180 nm diameter. The diameter of each tube was $<70$ nm [Fig. 2(a)]. The tube diameter is smaller than the patterned catalyst dot due to its "balling" at the growth temperature (600–700 °C).[8]

The high aspect ratio of the MWCNT increases drastically the effective electrode area compared to the substrate area used, greatly increasing capacitance without the need for a critical etching step. The $Si_3N_4$ layer appears to cover the MWCNT without any adhesion, pinhole, or step cover-

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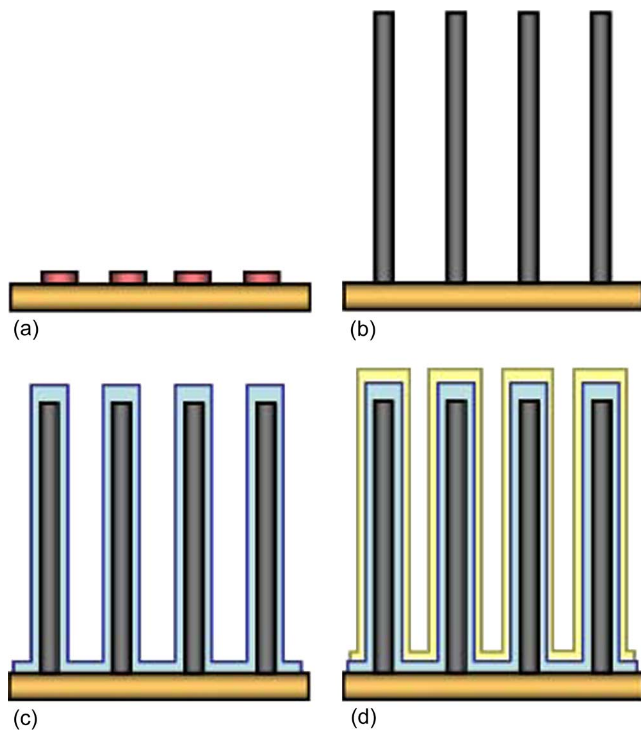



FIG. 1. A schematic illustration of MICNM capacitor structure. (a) The Nb bottom electrode was deposited by sputtering and the Ni catalyst dots were also formed on predefined locations. (b) The MWCNTs were vertically grown from the Ni catalyst dots using dc-PECVD. (c) The $Si_3N_4$ film was deposited by PECVD. (d) The Al layer was formed by angular thermal evaporation ($-45° - 45°$).

age problems with about 85 nm on the substrate and 65nm on the MWCNT wall [Fig. 2(b)]. Although the Al layer has some roughness due to angled evaporation, the SEM image shows proper step coverage with the Al layer on the $Si_3N_4$/MWCNT structure [Fig. 2(c)].

The capacitance and leakage current of various structures are shown in Fig. 3. Two different types of device were fabricated to compare with basic metal-insulator-metal (MIM) structures. One is where the Ni catalyst was patterned in a dot shape (<180 nm, diameter) with 1 $\mu$m pitch over a 200 $\mu$m $\times$ 200 $\mu$m area. The other has a line shape catalyst pattern, which has 180 nm width, 200 $\mu$m length, and 1 $\mu$m pitch over a distance of 200 $\mu$m (device area 200 $\mu$m $\times$ 200 $\mu$m as in the previous case). Figures 3(a) and 3(b) show vertically grown MWCNTs on these two different catalyst patterns. Most catalyst dots have a single MWCNT of about 3.5 $\mu$m height and 70 nm diameter. For the line catalyst pattern sample, a continuous line of MWCNTs (one or two tubes wide) occurs along the line pattern, akin to a row of trees in a plantation.[8] To make a capacitance structure, the $Si_3N_4$ and Al layers were formed by the fabrication process detailed earlier. The capacitance and leakage current, with varying applied bias, are shown in Figs. 3(c) and 3(d). The capacitance of the dot pattern and line pattern are about two and six times higher compared to an equivalent MIM struc-

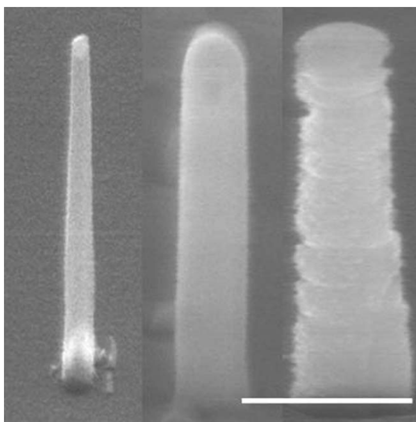
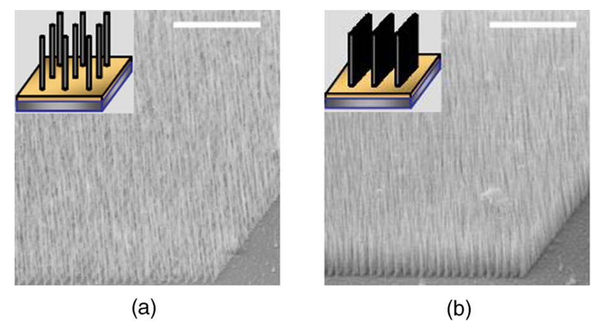
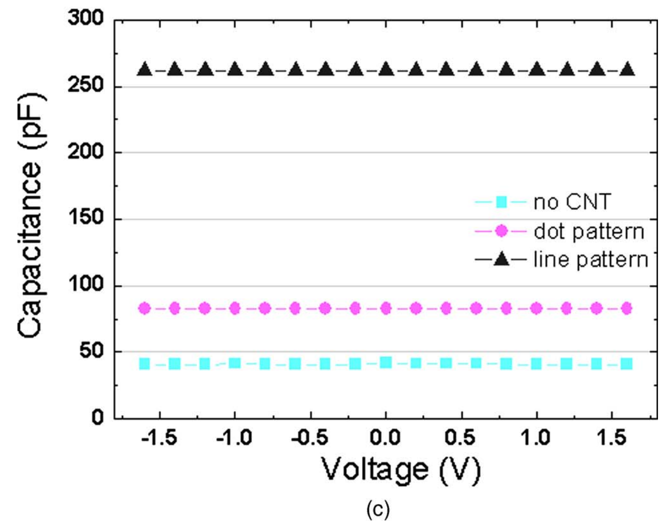


FIG. 2. SEM image of a single MICNM structure. (a) A single vertical MWCNT was grown on a selected position. (b) The $Si_3N_4$ layer was deposited on the MWCNT. (c) The Al layer was formed by angular evaporation. The scale bar corresponds to 500 nm.



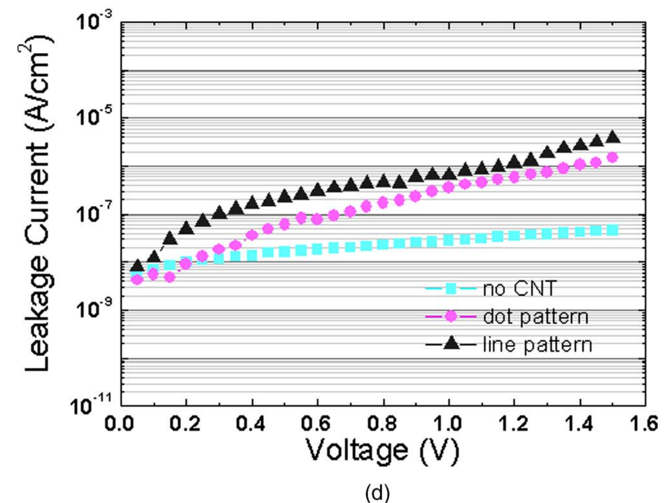




FIG. 3. SEM image and electrical characteristics of MICNM devices. (a) SEM image of MWCNTs on a dot catalyst pattern. (b) SEM image of MWCNTs on a line catalyst pattern. The scale bar corresponds to 10 $\mu$m. (c) Capacitance with varying applied bias. (d) Leakage current density with varying applied bias.

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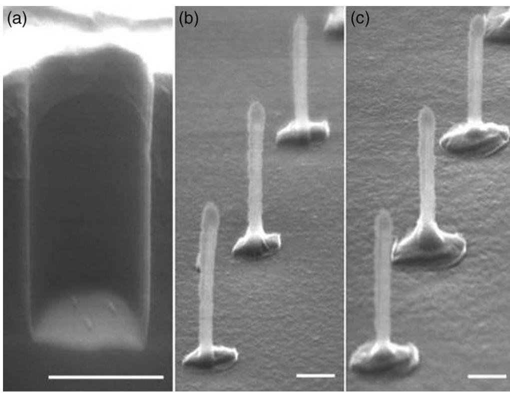


FIG. 4. SEM image of a nanoscale capacitor. (a) SEM image of an e-beam exposed pattern in thick PMMA resist. (b) Capacitor arrays using a 500 nm × 500 nm square pattern. (c) Capacitor arrays using a 1 $\mu$m diameter circle pattern. The scale bar corresponds to 500 nm.

ture in same area, even though, the area of the vertical capacitor occupies 1.8% and 11% of the substrate area, respectively. This is mainly due to an increase in the effective electrode area by the incorporation of vertical MWCNTs. The capacitance of the MICNM structure, employing a single MWCNT, can be approximated by a cylindrical capacitor model, $C=2\pi\varepsilon_0\varepsilon_r l/\ln(b/a)$, where $\varepsilon_0$ is permittivity in vacuum, $\varepsilon_r$ is the dielectric constant of $Si_3N_4$, $l$ is the nanotube length, $a$ is the nanotube diameter, and $b$ is the coaxial diameter of the $Si_3N_4$, respectively.[9,10] Using this model with $\varepsilon_0=8.85\times10^{-14}$F/cm, $\varepsilon_r=5.54$, $l\cong3.5$ $\mu$m, $a$ =70 nm, and $b$=200 nm, the capacitance of one MICNM structure is 1.027 fF, therefore, the total increase of capacitance by connecting 40 000 MICNM capacitors (200 $\mu$m × 200 $\mu$m/1 $\mu$m$^2$) in parallel is about 41 pF. For the line pattern sample, the capacitance is estimated by the planar capacitor model, $C=\varepsilon_0\varepsilon_r A/d$, where $A$ is the area of the electrode and $d$ is the thickness of $Si_3N_4$(65 nm), because the growth of the MWCNTs make a wall shape, and therefore, the side parts of the MWCNT surface contributes to the increase of effective electrode area, not the whole MWCNT surface, as shown in the inset of Fig. 3(b). The increase in the electrode area and capacitance by the incorporation of MWCNTs in this case is about $2.8\times10^{-7}$ m$^2$(=3.5 $\mu$m × 200 $\mu$m × 200 × 2) and 211 pF, respectively. The estimated values for the increase in capacitance ($\Delta C$) correspond extremely well with the experimentally measured values. The leakage current density is about 10 higher than in the standard MIM structure [Fig. 3(d)], however, there is no breakdown until 1.5 V, which is the normal driving voltage of present DRAMs. The leakage values are still acceptable for many applications.[3] The reason for the increase in the leakage current is likely to be associated with the greater difficulty of covering the MWCNT perfectly with the $Si_3N_4$ insulating layers, as the MWCNTs get closer to each other. Therefore, if two MWCNTs are grown from one catalyst or if MWCNTs are formed continuously with very narrow spacing between them, such as in the line pattern sample, the probability of having leakage paths is increased. Another reason is due to the structure effect of the device. A higher electrical field can be applied to the top of the capacitor due to the pointed shape of the MWCNT. The MIM capacitor has uniform field distribution on the structure in comparison.

Although the MICNM structure shows good electrical properties and the potential for high integration density, the high aspect ratio of this structure can be a problem for subsequent lithographic processes, where fine patterns are required. Electron beam lithography, commonly used for nanoscale patterning, can be a solution. Most e-beam lithography research, reported to date, has been based on using thin resist layers. However, it is possible to get fine pattern dimensions with a high aspect ratio in a thick resist layer, by using a high voltage electron beam (>40 K V).[11] Figure 4(a) shows a SEM image of a cross section of a patterned feature in 2-$\mu$m-thick poly(methylmethacrylate) (PMMA), after exposure at 1000 $\mu$C/cm$^2$ using a 50 pA probe current. The pattern size is about 500 nm and the wall shape is almost vertical. To pattern thicker resist layers, development time has to be increased. This longer developing time increases the pattern size by about 100 nm in diameter compared to the design size (400 nm). However, the final pattern size can be controlled by exposure bias. This result shows that e-beam lithography can be employed to pattern thick resist layers required to construct high aspect ratio vertical structures. The SEM images of a nanocapacitor array, fabricated using these e-beam lithography conditions, are shown in Figs. 4(b) and 4(c). The top electrode size is about 500 nm × 500 nm and 1 $\mu$m × 1 $\mu$m, respectively. Because the high resist wall makes a shadow effect during angular evaporation, the Al layer thickness of the top part is a little thicker than at the bottom of the MWCNT pillar. Nevertheless, the Al layer covers the $Si_3N_4$ coated MWCNT pillar structure well.

In summary, the successful fabrication of MICNM capacitors using vertically aligned MWCNTs is reported. The high aspect ratio of MWCNTs greatly increases the effective electrode area and, hence, the capacitance, very significantly. Fine patterning of the MICNM vertical structure has been achieved by using electron beam lithography with a resist layer of several micrometers thickness. The MICNM structure has the potential for replacing for the Si pillar structure in ultrahigh integration density DRAM. It also can be used more generally as a nanoscale capacitor, decreasing Si area consumed for capacitors in ultra large scale integration ICs.

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