Mechanism of radio-frequency current collapse in GaN–AlGaN field-effect transistors

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The mechanism of radio-frequency current collapse in GaN–AlGaN heterojunction field-effect transistors (HFETs) was investigated using a comparative study of HFET and metal–oxide–semiconductor HFET current–voltage ($I-V$) and transfer characteristics under dc and short-pulsed voltage biasing. Significant current collapse occurs when the gate voltage is pulsed, whereas under drain pulsing the $I-V$ curves are close to those in steady-state conditions. Contrary to previous reports, we conclude that the transverse electric field across the wide-band-gap barrier layer separating the gate and the channel rather than the gate or surface leakage currents or high-field effects in the gate–drain spacing is responsible for the current collapse. We find that the microwave power degradation in GaN–AlGaN HFETs can be explained by the difference between dc and pulsed $I-V$ characteristics. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1363694]

GaN-based heterojunction field-effect transistors (HFETs) demonstrate record levels of carrier density in two-dimensional electron gas (2DEG) layers at the GaN–AlGaN interface. Nowadays sheet carrier concentration in 2DEG exceeding $10^{13}\,\mathrm{cm}^{-2}$ with room-temperature mobility above 1000 $\mathrm{cm}^2/\mathrm{V\,s}$ can be routinely obtained. These values yield saturation current of 0.5–0.7 A/mm (Ref. 1) and cutoff frequency (f_T) approaching 100 GHz for submicron gate devices. We have recently demonstrated that the maximum saturation current can be further increased, with no degradation in f_T, by using metal–oxide–semiconductor HFET (MOSHFET) device structures.[2] This allows up to +10 V of gate bias and a maximum current of 1.3 A/mm for a device with a 1.5-μm-long gate. Furthermore, a maximum current of more than 5 A from a single-multigate on-wafer MOSHFET was also measured and reported recently.[3] These extremely high channel currents in conjunction with breakdown voltages above 100 V, suggest the possibility of obtaining record high microwave output powers in GaN–AlGaN field-effect transistors (FETs). A maximum rf output power in a class-A amplifier mode should be about

$$(1.3\mathrm{A/mm})100\mathrm{V}/8=16.25\ \ \mathrm{w/mm}$$

for MOSHFETs and about

$$(0.7\mathrm{A/mm})100\mathrm{V}/8=8.75\ \ \mathrm{w/mm}$$

for HFETs. However, both GaN–AlGaN HFETs and MOSHFETs still demonstrate typical rf output powers of about 3–5 W/mm, even under pulsed bias conditions that eliminate heating effects. The phenomenon responsible for this degradation is generally referred as ''rf-current collapse'' or ''current slump,'' which recently has been a subject of several studies.[4–9] Drain currents under large input drives were measured showing significant current compression compared to the dc values.[4,5,8] Activation energies of deep traps responsible for the current collapse were studied by optical and thermoexcitation methods.[6,7] The surface passivation approach was suggested to increase the microwave output power.[9,10] However, although the current collapse phenomenon seems to be general for different types of GaN–AlGaN FETs, as well as for GaAs power FETs, both the concrete mechanism of rf output power suppression and physical locations of the carrier trapping centers responsible for the collapse, are still far from clear.

In this letter, we compare the $I-V$ and transfer characteristics for HFETs and MOSHFETs, which were measured under dc steady-state voltages, and under short voltage pulses applied either to the drain or to the gate. A severe current collapse in gate pulsed mode measurement was observed for both device types at low (below the knee voltage) and high drain biases. We then used the measured $I-V$ curves to simulate (via Fourier analysis) the variations in dc and rf-current components as functions of the input rf-signal amplitudes at different gate biases. By comparing experimental results and simulations, we further show that the difference between dc and pulsed $I-V$ characteristic explains the microwave power degradation in GaN–AlGaN FETs.

The device epilayer structure was grown by low-pressure metal–organic chemical-vapor deposition over 4H–SiC substrates (see Ref. 2 for a more detailed description). The heterostructure consists of a 1 μm insulating GaN layer capped with a 30 nm $Al_{0.2}Ga_{0.8}N$ barrier layer, which was doped with silicon approximately to $2\times10^{18}\,\mathrm{cm}^{-3}$. The measured room-temperature Hall mobility and sheet carrier concentration were 1150 $\mathrm{cm}^2/\mathrm{V\,s}$ and $1.2\times10^{13}\,\mathrm{cm}^{-2}$, respectively.

Prior to the gate fabrication, a 15 nm SiO_2 layer was deposited on part of the heterostructure using plasma-

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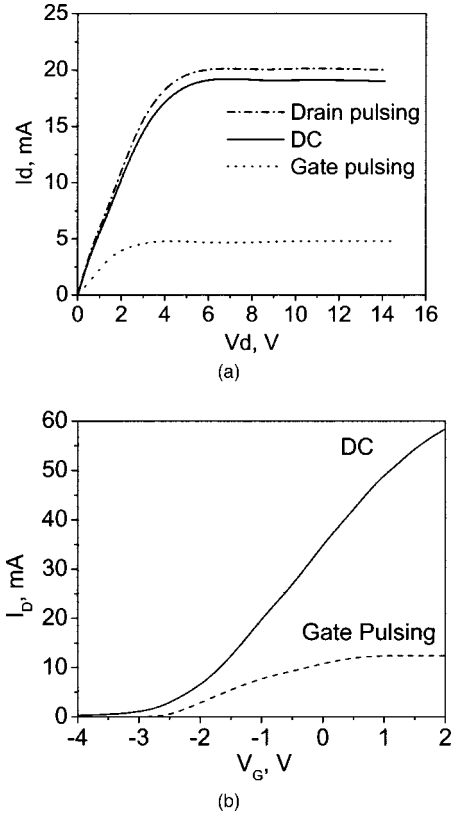

FIG. 1. Measured GaN–AlGaN HFET characteristics: (a) $I-V$ characteristic in dc, drain, and gate-pulsed modes at -1 V gate bias; and (b) transfer characteristic in dc and gate-pulsed modes at 15 V drain bias.

enhanced chemical-vapor deposition. The SiO_2 layer was used to fabricate MOSHFETs on the same wafer along with regular HFETs. The devices used in the experiments had a drain–source opening of 5 μm, gate length of 1.5 μm, and a gate width of 50 μm. A small gate width was chosen to reduce the heating effects.

The HFETs demonstrated the saturation current of 0.6 A/mm (at zero gate bias) and the threshold voltage of -4 V. For the MOSHFET, the saturation current reached approximately 1 A/mm at $+3$ V gate bias and the threshold voltage was -7 V. Typical HFET dc $I-V$ characteristic at -1 V gate bias are shown by the solid line in Fig. 1(a). Figure 1(b) shows the transfer characteristic of the same device measured at $+15$ V drain bias. The dashed-dot lines in Fig. 1 show the $I-V$ and transfer curves measured when 1 μs voltage pulses were applied to the drain. As can be seen, these pulsed characteristics are very close to the dc ones. This demonstrates that HFETs do not exhibit either heating effects or current collapse in the drain-pulsing mode. We then measured the $I-V$ and transfer characteristics for the same device by applying 1 μs voltage pulses to the gate. These characteristics are shown by the dashed lines in Fig. 1. The minimum value of pulsed voltage was close to the HFET's threshold value, while the peak voltage was varied. A significant current collapse in the gate pulsing mode is evident from Fig. 1. The same difference between dc and gate pulsed $I-V$ was found in MOSHFET devices from the same wafer. Several important conclusions can be reached by analyzing these pulsed $I-V$ characteristics.

(i) Since the gate leakage current in MOSHFETs is about 4–6 orders less than that in HFETs,[3] the gate leakage current as the mechanism responsible for current collapse can be ruled out. Also, since the surface conditions are quite different for HFETs and MOSHFETs, we believe that surface states in the source–gate–drain openings do not contribute significantly to the current collapse. This is contrary to the conclusions of past researchers.[9,10]

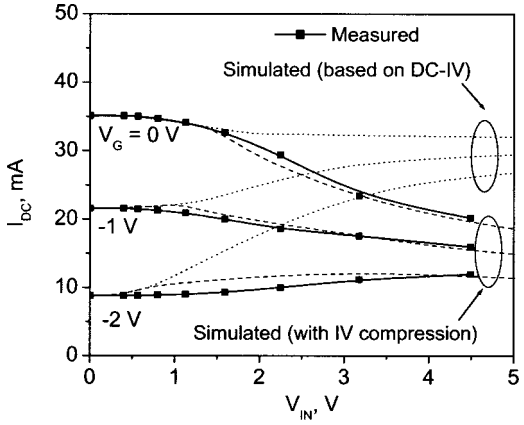

FIG. 2. Measured (solid lines) and simulated (dashed and dashed-dotted lines) dc current components as a function of input rf signal amplitude at 15 V drain bias and different gate biases.

(ii) The current compression in gate-pulsed mode occurs both at low (below the knee voltage) and high drain bias [Fig. 1(a)]. This means that the high-field domain between gate and drain cannot cause the collapse.

(iii) Although the lateral electric field between the gate and drain has the same time dependence and amplitude in both drain- and gate-pulsed modes, the current collapse occurs only in the gate-pulsing mode. Thus, we conclude that the transverse field across the gate-to-channel barrier layer, rather than the lateral field in the gate–drain spacing is responsible for the carrier trapping. The magnitude of the current compression was found to be roughly proportional to the gate voltage swing. This collaborates our conclusion.

A more detailed discussion of the physics of the current collapse will be published elsewhere.

On the wafer, rf measurements were performed at 2 GHz using a HP8341B rf generator and a HP83020A rf power amplifier. Transistors were connected to the rf signal source and load using Cascade microwave probes. The output rf power and dc component of the FET current were measured as functions of the input rf power at 15 V drain bias. The amplitude of the input voltage was calculated from the measured incident and reflected rf power values. A load pull tuning using the MAURY automated tuner system was performed in order to optimize the output rf power. The solid line in Fig. 2 shows the measured dependence of the dc current component on the input signal amplitude.

Using a computer simulation, a 2 GHz rf signal was weighted by the device transfer curve of Fig. 1(b) at gate biases of -2, -1, and 0 V. The Fourier analysis was then used to calculate the dc current component as a function of the input rf amplitude at the gate for different gate biases. These simulated dependencies based on the dc transfer characteristics are shown by the dotted lines in Fig. 2. As can be seen, the device dc current changes significantly as a function of the rf input drive. At a low gate bias, an increase in

the input signal causes an increase in the dc current component due to the current cutoff during the time when the total device voltage is below threshold. On the contrary, at a high gate bias, the dc current component decreases with an increase in input signal due to the current saturation at high peak input voltage.

It is worth mentioning here that the same type of dc current dependencies were recently measured and discussed by Nguyen, Nguyen, and Grider.[4] These authors attributed the observed current compression to carrier trapping in the device channel. It is obvious, however, from Fig. 2 that even in the absence of any trapping, the dc current component depends significantly on the input signal. The effect of traps and collapse in current becomes evident by comparing the simulated curve discussed above at -1 V gate bias with the measured characteristics at the same gate bias. When the input rf drive is zero, the FET's operating point corresponds to its transfer dc $I-V$ of Fig. 1(b). At low levels of the rf input signal, the transfer characteristic remains undistorted. With the continuous increase in the rf drive, the voltage swing across the gate increases. When this voltage swing becomes large enough, the dc transfer curve of the device starts to collapse, corresponding to a decrease in current. Due to this collapse, a further increase in the input signal shifts the transfer characteristic down and the operating point moves gradually from its dc $I-V$ position to the point on the gate-pulsed $I-V$ curve corresponding to the same gate voltage. The dashed curves in Fig. 2 were simulated using the transfer characteristic of Fig. 1(b) gradually transforming, from dc $I-V$ to pulsed $I-V$ as the value of the input signal increases. As seen from Fig. 2, the simulation accounting for the changes of the transfer characteristic agrees very closely with the experimental results.

Provided that output load impedance is optimized, the rf output power at a dc drain voltage V_d can be estimated as

$$P_{\mathrm{ac}}=[I_{\mathrm{ac}}(V_d-V_{\mathrm{knee}})]/2\,,$$

where V_{knee} is the knee voltage of the HFET $I-V$ curve. This equation was used to extract the rf-current amplitude from the output power measurements. The dependence of the measured rf-current amplitude on the input voltage is shown by the solid line in Fig. 3. Figure 3 also shows the rf-current harmonic amplitudes calculated using the Fourier-based simulations based on the dc $I-V$ curve (dotted line), and accounting for the transfer curve compression with an increase in the rf input swing. As can be seen, the simulations accounting for the current compression describe the experimental results quite accurately. On the other hand, the simulations based on the dc transfer curve predict a much higher output rf power (see Fig. 3).

In conclusion, we have demonstrated that the current collapse responsible for the degradation of rf power of GaN–AlGaN HFETs and MOSHFETs occurs when the electric field between the gate and the channel changes due to applied gate voltage swing. This change causes the change in the trapped charge beneath the gate and results in compression of the transistor transfer characteristic. The simulations of the dc and rf current components accounting for this input rf-signal-dependent compression agree very closely with our experimental data.

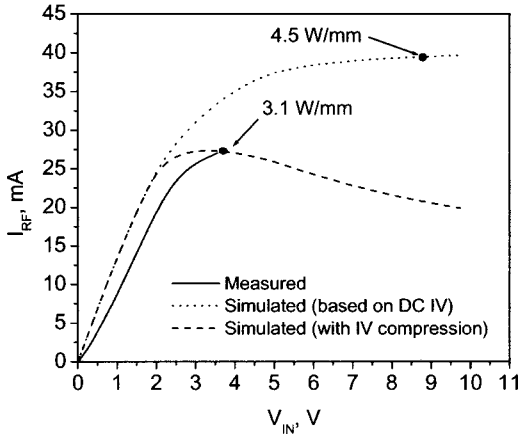

FIG. 3. Measured (solid lines) and simulated (dashed and dashed-dotted lines) rf current amplitudes vs input rf-signal amplitude at -1 V gate bias. The output power of 3.1 W/mm was measured for this device at 15 V drain bias. The output power calculated from the simulated current amplitude is also shown.

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