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Temperature behaviour of electron mobility in double-gate silicon on insulator transistors

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Abstract

We have studied the electron mobility behaviour in double-gate silicon on insulator (DGSOI) inversion layers as a function of temperature. It has been shown that as in the case of room temperature, volume inversion plays a very important role, being responsible for the enhancement of the electron mobility in a certain range of silicon thicknesses, T_w. Poisson's and Schrödinger's equations have been self-consistently solved to study the distribution of the electrons in DGSOI structures as a function of temperature. As in the room temperature case, volume inversion means that in the range of silicon thicknesses between 5 nm and 20 nm, the phonon-scattering rate is lower than the corresponding value for bulk silicon inversion layers. We have solved the Boltzmann transport equation by the Monte Carlo method, and have evaluated the electron mobility. For the whole range of temperatures we observed that for 5 nm $< T_w <$ 20 nm, electron mobility in DGSOI devices, μ_{DGSOI}, is higher than the mobility for bulk silicon inversion layers, μ_{bulk}, and that the factor $\frac{\mu_{\mathrm{DGSOI}}}{\mu_{\mathrm{bulk}}}$ increases as the temperature decreases, i.e., the improvement of the mobility due to the volume inversion effect is more important at low temperatures than at room temperature.

1. Introduction

A double-gate silicon on insulator (DGSOI) structure consists, basically, of a silicon slab sandwiched between two oxide layers. A metal or polysilicon film is deposited on each oxide [1]. Each of these films then acts as a gate electrode (front and back gate), which is capable of generating an inversion region near the two Si–SiO_2 interfaces, if the appropriate bias is applied. Thus, two metal oxide semiconductor field effect transitors (MOSFETs) would be sharing the substrate, the source and the drain. However, the main feature of these structures arises from the concept of volume inversion, introduced and demonstrated some time ago by Balestra *et al* [2, 3] by simultaneously biasing the two gates of a fully depleted (FD) SOI transistor: if the Si film is thicker than the sum of the depletion regions induced by the two gates, no interaction is produced between the two inversion layers, and the operation of this device is similar to that of two conventional MOSFETs connected in parallel. However, if the Si thickness is sufficiently reduced, the whole silicon film is depleted and an important degree of interaction takes place between the two potential wells. In such conditions the inversion layer is formed not only at the top and bottom of the silicon slab (i.e., near the two silicon–oxide interfaces), but throughout the entire silicon film thickness. The device is then said to operate in volume inversion, i.e., the carriers are no longer confined to one interface, but are distributed throughout the entire silicon volume. Several authors have claimed that volume inversion presents a significant number of advantages, such as: (i) an enhancement of the number of minority carriers; (ii) an increase in carrier mobility and velocity due to reduced influence of the scattering associated with oxide and interface charges and surface roughness; (iii) as a consequence of the latter, an increase in drain current and transconductance; (iv) a decrease in low-frequency noise; (v) a great reduction in hot carrier effects and (vi) a steep

subthreshold slope [2, 3]. In addition, like other dual-gated devices, DGMOSFETs are claimed to be more immune to short channel effects (SCEs) than bulk silicon MOSFETs and even single-gate fully depleted SOI MOSFETs [1]. This is due to the fact that the two gate electrodes jointly control the carriers, thus screening the drain field away from the channel [4]. This characteristic would permit a much greater scaling down of these devices than ever imagined for conventional MOSFETs [5].

In previous works [6, 7], we studied the electron mobility in a DGSOI device as a function of the transverse effective field and silicon layer thickness at room temperature. The contributions of the main scattering mechanisms (phonon scattering, surface-roughness scattering due to both Si–SiO_2 interfaces, and Coulomb interaction with the interface traps of both interfaces) were taken into account and carefully analysed. We demonstrated that the contribution of surface scattering mechanisms is by no means negligible; In contrast it plays a very important role which must be taken into account when calculating the mobility in these structures. We show that two opposite trends appear with respect to electron mobility as the silicon thickness is reduced.

(i) On the one hand, the subband-modulation effect [8], produced by the splitting of the degeneracy of the silicon conduction band due to size quantization. The subband-modulation effect produces a greater separation between the energy subbands of non-primed and primed valleys [9], and consequently a redistribution of the electrons among the different subbands, which causes an increase in the population of non-primed subbands at the expense of the population of primed subbands, which logically decreases. As the conduction effective mass of electrons in non-primed valleys is lower ($0.190m_0$, m_0 being the electron free mass) than the conduction effective mass of electrons in primed valleys ($0.315m_0$), an initial effect of subband modulation is a decrease in the average conduction effective mass of the electrons. The subband-modulation effect also produces a reduction in the intervalley scattering rate among non-equivalent valleys, produced by the greater energy separation between primed and non-primed subbands. Both effects facilitate electron transport, and therefore contribute to an increase in the mobility.

(ii) On the other hand, the reduction in the silicon thickness produces a greater confinement of the carriers and taking into account the uncertainty principle, an increase in the phonon-scattering rate [10], which impedes electron transport, and therefore, contributes to a decrease in the mobility. However, it has been shown that for DGSOI inversion layers at room temperature, in the range 5–20 nm (this range depends on the inversion electron density, N_{inv}) phonon scattering decreases instead of increasing, and a phonon-scattering rate lower than that for bulk silicon inversion layers is obtained [6, 11, 12].

In summary, two opposite effects simultaneously affect the electron mobility of the electrons in DGSOI inversion layers. The variation in electron mobility in DGSOI devices as T_w decreases was compared with that in single-gate silicon on insulator structures and in bulk silicon inversion layers (i) when only phonon scattering was considered, (ii) when the effect of surface-roughness scattering was taken into account and (iii) when the contribution of Coulomb interaction with charges trapped at both interfaces was taken into consideration (in addition to phonon and surface-roughness scattering). From this comparison we determined (in the above three cases) the existence of the following three regions: (i) an initial region for thick silicon layers ($T_w > 20$–30 nm), where the mobility for both structures tends to coincide, approaching the bulk value. (ii) As T_w decreases we show that volume inversion modifies the electron transport properties by reducing the effect of all scattering mechanisms. Accordingly, the electron mobility in DGSOI inversion layers increases by an important factor which depends on the silicon thickness and the transverse effective field. (iii) Finally, for very small thicknesses, the limitations to electron transport are due to geometrical effects, and therefore the two mobility curves, which again coincide, fall abruptly. We show the existence of a range of thicknesses of a silicon layer (between 5 nm and 20 nm) in which electron mobility is improved by 25% or more, due to volume inversion. Therefore, volume inversion plays an important role in the electron mobility in these DGSOI devices as the silicon thickness is reduced below 20 nm.

Therefore, the distribution of the electrons in the silicon layer plays a very important role in the determination of transport properties. It is well known that the distribution of the electrons in inversion layers varies greatly with temperature changes [9]. We speculated whether this mobility behaviour at room temperature is modified as the temperature decreases. For example, *a priori*, it is well known that as temperature decreases, quantum-size effects become more important, even for bulk silicon inversion layers, where at low temperatures the population of electrons in non-primed subbands is very high. As shown by Ando *et al* [9] the fraction of the electrons in the non-primed subbands in a bulk silicon inversion layer is 1 for very low temperatures. This means, for example, that the influence of subband-modulation effects becomes weaker and weaker as the temperature is reduced.

To shed some light on the above question, we have made an in-depth study of the temperature behaviour of electron mobility in DGSOI devices. To do so, we followed a procedure similar to that adopted in [6] to study DGSOI devices at room temperature. Thus, we used a one-electron Monte Carlo method to study the stationary electron transport properties in asymmetric DGSOI inversion layers, focusing our attention on the evaluation of the stationary drift velocity and the low-field mobility at room temperature. Electron quantization in the inversion layer was appropriately taken into account, and Poisson's and Schrödinger's equations were self-consistently solved assuming a simple non-parabolic band model for the silicon. Once the electron distribution in the silicon layer had been determined, the Boltzmann transport equation was solved by the Monte Carlo method, simultaneously taking into account phonon- and surface-roughness scattering. As demonstrated previously [6, 7, 13–15], the presence of two close silicon–oxide interfaces in both single- and double-gate SOI MOSFETs produces a significant difference with respect to their standard-bulk counterparts. Therefore, we had to develop improved models capable of taking into account the effect of the roughness of both interfaces [7, 13] on the total scattering rate, and models to calculate the Coulomb scattering rate in ultrathin SOI structures [15], which have been

shown to be different from the models used for conventional silicon bulk inversion layers. We considered n-channel DGSOI MOSFETs with different values of silicon thickness and different temperatures. The distribution of the electrons was evaluated by self-consistently solving the Poisson and Schrödinger equations. The role of volume inversion as the temperature is reduced is investigated in section 2. Electron mobility curves for DGSOI MOSFETs are evaluated in section 3 using a one-electron Monte Carlo simulator to solve the Boltzmann transport equation for different values of the silicon thickness, and for different temperatures. The relation between electron mobility, silicon thickness and temperature is shown. Finally, the main conclusions of this work are drawn in section 4.

2. Electron distribution and Poisson and Schrödinger solution

The structure we have considered consists of a lightly doped ($N_A = 1 \times 10^{15}$ cm^{-3}) silicon layer sandwiched between two oxide layers 1 nm thick ($t_{ox} = 1$ nm). Two polycrystalline silicon (polysilicon) gates were assumed as control electrodes. The front upper and back lower gates were n$^+$- doped ($N_{D\text{-poly}} = 1 \times 10^{20}$ cm^{-3}) and the same gate voltage was applied simultaneously to both gates ($V_{G1} = V_{G2} \equiv V_G$). Different silicon layer thicknesses, ranging from $T_w = 1.5$ nm to $T_w = 50.0$ nm, were considered. We assumed that the silicon layer was left undoped. In a DGMOSFET, short channel effects are controlled by device geometry [4, 5], whereas in a bulk FET the short channel effects are controlled by doping (channel doping and/or halo doping). Therefore, in principle, the channel of a DGMOSFET can be undoped, which allows better carrier transport and avoids threshold voltage fluctuation due to discrete, random dopant placement.

Quantum size effects are known to become very important in these devices (since carriers are confined by the silicon thickness, which is comparable to the De Broglie wavelength of the carriers) and therefore, the self-consistent solution of Poisson's and Schrödinger's equations is required to evaluate the spatial distribution of the electrons in the silicon layer. To solve Poisson's equation, we considered a non-uniform adaptive mesh, employing an iterative-Newton scheme. The actual band-bending through the whole structure and the finite height of the barrier at the Si–SiO$_2$ interfaces were considered. A non-parabolic band model for the silicon was taken into account assuming $\alpha = 0.5$ eV, where α is the parameter of non-parabolicity [16]. This limited our study to low-electron energies (below 0.5 eV). The effective electron masses were assumed to be those of bulk silicon [6, 18].

Figure 1 shows the electron distribution, $n(z)$, throughout the silicon layer in a DGSOI inversion layer for a silicon thickness of $T_w = 5.0$ nm, for different temperatures. The inversion charge concentration, N_{inv}, defined here as

$$N_{\text{inv}} = \int_0^{\frac{T_w}{2}} n(z)\,\mathrm{d}z \tag{1}$$

was fixed at $N_{\text{inv}} = 5 \times 10^{12}$ cm^{-2}. Note that electron distribution strongly depends on the temperature, and therefore, so do the transport properties.

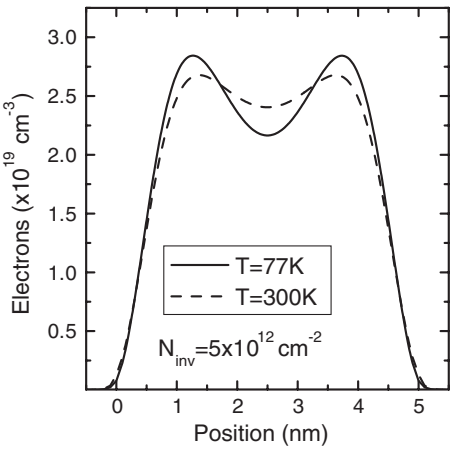

Figure 1. Electron distribution in a double gate silicon on insulator transistor for two temperature values: $T = 77$ K (solid line) and $T = 300$ K (dashed line). Gate bias was set to get an inversion charge concentration of $N_{\text{inv}} = 5 \times 10^{12}$ cm^{-2}.

2.1. Subband-modulation effect

As mentioned above, the first consequence of the subband-modulation effect is related to the redistribution of the carriers among the different electric subbands originated by size quantization [6, 14]. The self-consistent solution of the Poisson and Schrödinger equations in an SOI inversion layer shows that the separation between the energy levels of the two subband ladders produced by the splitting of the degeneration of the silicon valleys, as a consequence of size quantization, increases as the thickness of the silicon layer is reduced. An important consequence of this fact is that the population of non-primed subbands increases at the expense of the primed subband population as the silicon layer thickness is reduced [9]. However, at low temperatures (even for bulk silicon inversion layers) electrons already mainly populate non-primed subbands, and so at a given temperature, the evolution of the subband population with the silicon thickness is smoother than that at room temperature. Figure 2 shows the variation in the populations of non-primed subbands and primed subbands as a function of the silicon thickness for different temperatures. Note that the lower the temperature, the higher the population of non-primed subbands (regardless of the silicon layer thickness). As a result, a lower conduction effective mass is expected as the temperature is reduced, for a given silicon thickness. Figure 3 shows the changes in the conduction effective mass for different temperatures. According to the above discussion, the lower the temperature, the lower the average conduction effective mass.

2.2. Phonon-scattering increase

Another important effect that appears in SOI inversion layers with decreasing thickness of the silicon layer is an increase in the phonon-scattering rate [6, 14]. Due to the presence of the second Si–SiO$_2$ interface, uncertainty concerning the location of the electrons in the direction perpendicular to the interface is lower in SOI samples than in bulk samples. By the uncertainty principle, there is a wider distribution of the electron's momentum perpendicular to the interface. In

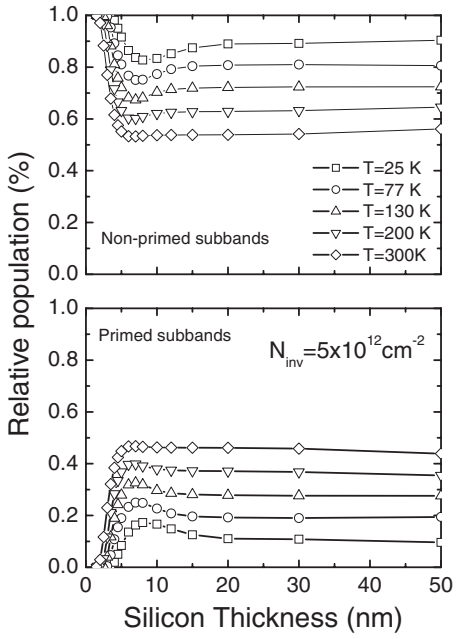

Figure 2. Relative populations of non-primed and primed subbands in a DGSOI inversion layer as a function of the silicon thickness for different temperatures. The inversion charge concentration was taken as $N_{\text{inv}} = 5 \times 10^{12}$ cm^{-2}.

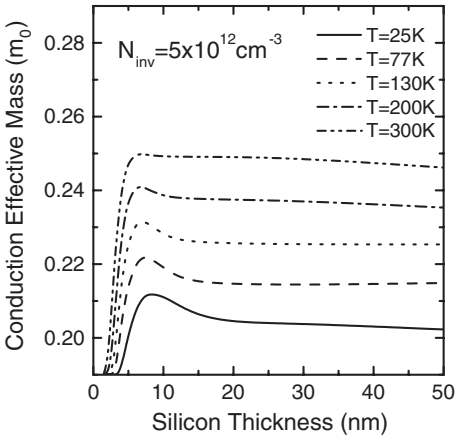

Figure 3. Average conduction effective mass for electrons in a DGSOI inversion layer as a function of the silicon thickness for different temperatures. The inversion charge concentration was taken as $N_{\text{inv}} = 5 \times 10^{12}$ cm^{-2}.

other words, due to size quantization, the electron's interface-directed momentum does not have a single value (as in three-dimensional electrons), but rather a distribution of likely values that expands as the silicon layer thickness is reduced. Taking into account momentum conservation, there are more bulk phonons available that can assist the transitions between electronic states, and therefore the phonon scattering increases. Thus for the same inversion-charge concentration, the phonon-scattering rate is greater in thinner films than in thicker ones (since the confinement is greater), and therefore we expect a reduction in the mobility. Numerically, this effect is reflected in the following form factor:

$$I_{\mu\nu} = \int_{-\infty}^{\infty} |\psi_\mu(z)|^2 |\psi_\nu(z)|^2 \, \mathrm{d}z \qquad (2)$$

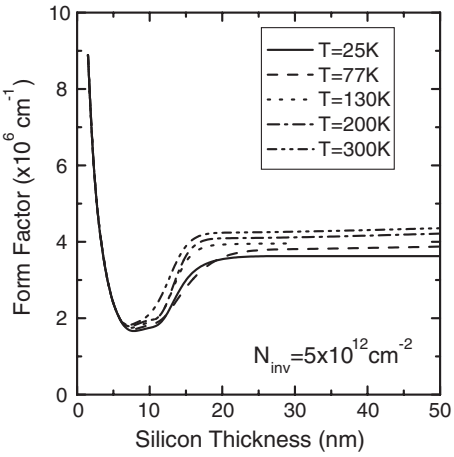

Figure 4. Form factor for the ground subband in a DGSOI inversion layer as a function of the silicon thickness for different temperatures. The inversion charge concentration was taken as $N_{\text{inv}} = 5 \times 10^{12}$ cm^{-2}.

which multiplies the phonon-scattering rates [10], where $\psi_\nu(z)$ is the envelope of the electron wavefunction in the direction perpendicular to the interface in the νth subband. When confinement is greater (the overlap integral of the envelope wavefunctions is also larger) the phonon-scattering rate increases.

However, in DGSOI devices at room temperature, we have shown that volume inversion means that in the range 5–20 nm, the phonon-scattering rate decreases instead of increasing [6]. Figure 4 shows the above form factor for the ground subband ($\mu = \nu = 0$) for different temperatures. Note that all the curves, regardless of the temperature, show a similar behaviour: for thinner samples the form factor is very large due to the geometrical confinement of electrons in a very narrow space. As the silicon slab thickness increases, the form factor is quickly reduced, until a minimum is reached in the region between 5 and 15 nm. Then, it increases to approach, for thick samples ($T_w > 20$ nm), the value presented in bulk silicon inversion layers. As can be seen in the figure, in the range $T_w = 5 \rightarrow 15$ nm the form factor for DGSOI is lower than that corresponding to bulk inversion layers ($T_w \rightarrow \infty$). Consequently, in this range the phonon-scattering rate in the DGSOI inversion layer decreases, instead of increasing as expected. This is an important result, a direct consequence of the volume inversion effect. Thus, we show that there exists a range of silicon layer thicknesses where electron mobility for DGSOI inversion layers is greater than that for bulk inversion layers [6]. It should be noted, however, that this behaviour is more acute as temperature decreases.

3. Electron mobility

To study variations in electron mobility behaviour in DGSOI inversion layers as the temperature varies, we used a one-electron Monte Carlo simulator, developed and described elsewhere [13, 14]. Phonon- and surface-roughness scattering have been taken into account in this work. We used bulk electron–phonon scattering models, considering acoustic deformation potential scattering and intervalley scattering

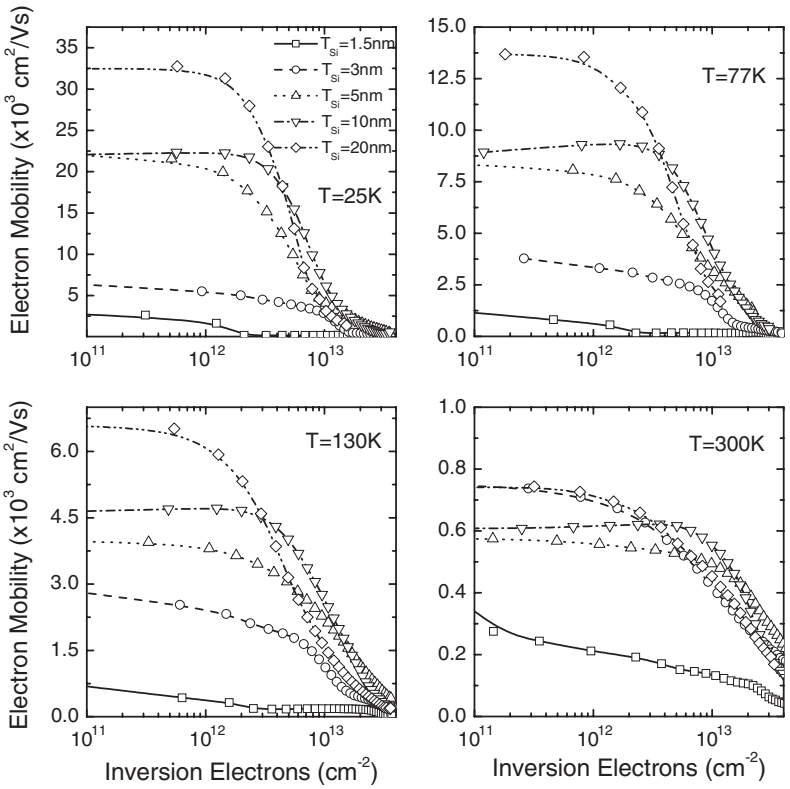

Figure 5. Electron mobility curves in a DGSOI inversion layer as a function of N_{inv} for different temperatures.

(between both equivalent and non-equivalent valleys). The coupling constants for the intervalley phonons and the acoustic deformation potential are the same as in bulk silicon inversion layers [17, 18]. The phonon-scattering rates for inversion layers were deduced by using Price's formulation [10]. Here again, the use of bulk phonons is questionable, as the presence of Si–SiO_2 interfaces undoubtedly alters the dispersion of the phonons, their nature and their coupling to the electrons. Previous studies [19] accounting for these effects in idealized conditions showed that phonon-limited mobility is reduced by 20% or less [17] due to the presence of the Si–SiO_2 interfaces. Nevertheless, if such idealized conditions are relaxed, an even lower reduction is expected. For these reasons and due to the difficulty in dealing with the effects of the interfaces on the phonon-scattering rate [17, 19], we have assumed that the bulk phonons are not influenced by the layered structure. In any case, the presence of the two Si–SiO_2 interfaces becomes more important as the silicon layer thickness is reduced. This effect will be the object of future studies. Finally, the effect of SiO_2 polar-phonon remote scattering has also been ignored. Very recently, Fischetti *et al* [20] have shown that the effect of polar-phonon remote scattering could be important at high transverse effective fields (or high inversion charge concentrations) if very thin (<2 nm) oxide layers are used. In this simulation, the electron energy was limited to 0.5 eV, since for higher electron energies the results obtained by the simulation are not likely to be very accurate, as a detailed bandstructure was not used. Accordingly, as the silicon bandgap was set to 1.12 eV at room temperature (thus setting the energy threshold for the impact ionization process), impact ionization was not included. If the scattering mechanisms related to the presence of the Si–SiO_2 interface significantly affect the electron transport properties in bulk silicon inversion layers [17], one can easily understand that this effect should, at least *a priori*, be taken into account in those physical systems where electrons are simultaneously affected by two such Si–SiO_2 interfaces. Such is the case of the ultrathin DGSOI inversion layers studied here. It has recently been proved that in ultrathin single-gate SOI (SGSOI) [13] and in DGSOI [6, 7] inversion layer devices, the presence of a second interface plays a very important role, both by modifying the surface-roughness scattering rate due to the gate interface, and by providing a non-negligible scattering rate [13]. On the other hand, the usual surface-roughness scattering model in bulk silicon inversion layers has been shown to overestimate the effect of surface-roughness scattering arising from one of the interfaces as a consequence of the presence of the other. Therefore, it was necessary to improve the surface-roughness model in order to calculate the scattering rate due to both interfaces (which are assumed not to be correlated). Such a model is detailed in [13] and [7]. Although the latter model was developed for SGSOI devices, no assumption was made explicitly involving such a structure. This means that the model is a general one and therefore may be applied to the case of the DGSOI devices.

By using this simulator, we were able to calculate the electron mobility in DGSOI inversion layers for different silicon film thicknesses (T_w). Our attention was focused on evaluating the stationary drift velocity and the low-field mobility. A comprehensive description of this simulator can be found elsewhere [14, 21–24].

Figure 5 shows electron mobility curves versus the inversion charge sheet for different values of silicon thickness.

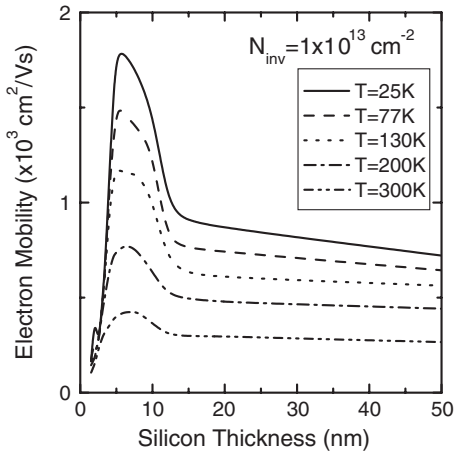

Figure 6. Evolution of the electron mobility in a DGSOI inversion layer with the silicon thickness for different mobility values ($N_{\rm inv} = 1 \times 10^{13}$ cm^{-2}).

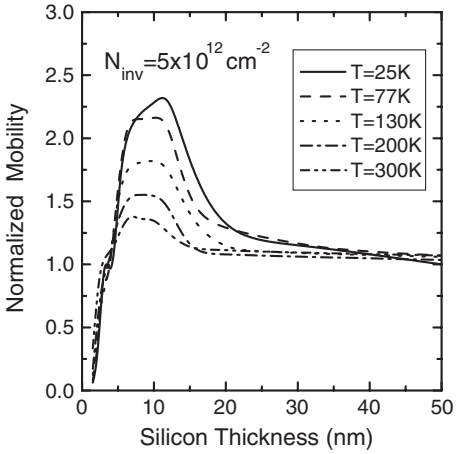

Figure 7. Evolution of the factor $\frac{\mu_{\rm DGSOI}}{\mu_{\rm bulk}}$ with the silicon thickness for different temperatures, $\mu_{\rm DGSOI}$ being the mobility for a silicon inversion layer with a silicon thickness T_w and $\mu_{\rm bulk}$ the electron mobility in a bulk silicon inversion layer at the same temperature.

Different temperatures were considered, namely $T = 25$ K, 77 K, 130 K and 300 K. It can be observed that, for all the temperatures considered, there is more than one trend in the electron mobility as the silicon thickness decreases. In addition, this trend strongly depends on the inversion electron density. To see this more clearly, figure 6 shows the evolution of the mobility with the silicon layer thickness for the temperatures considered in this study. Note that all the curves present the shape described in the Introduction for the behaviour of the mobility in DGSOI devices at room temperature, i.e., there are three different regions: (i) an initial region for thick silicon layers ($T_w >$ 20–30 nm), where mobility decreases as T_w increases and approaches the bulk value. (ii) As T_w decreases we show that volume inversion modifies the electron transport properties by reducing the effect of all scattering mechanisms. Accordingly, the electron mobility in DGSOI inversion layers increases by an important factor which depends on the silicon thickness, the transverse effective field and the temperature. (iii) Finally, for very small thicknesses, the limitations to electron transport are due to geometrical effects, and therefore the mobility curves fall abruptly for all temperatures. To obtain a clearer idea of the effect of volume inversion, we have normalized each mobility curve shown in figure 6 by the corresponding value of the mobility in a bulk silicon inversion layer at the same temperature. The results of this are shown in figure 7. As can be observed, the improvement in the mobility in a DGSOI inversion layer, $\mu_{\rm DGSOI}$, with regard to the mobility in a bulk silicon inversion layer, $\mu_{\rm bulk}$, is greater as the temperature is reduced: the maximum improvement, $\frac{\mu_{\rm DGSOI}}{\mu_{\rm bulk}}$, is 1.35 at room temperature for $T_w = 10$ nm, this quotient reaching 2.33 for $T = 25$ K for the same silicon thickness.

4. Conclusions

We have analysed the behaviour of electron mobility in DGSOI inversion layers as a function of temperature. We have observed that at lower temperatures, electron mobility versus the silicon layer thickness reduction behaves in a similar way to what is found at room temperature, i.e. three different regions can be distinguished: (i) for high values of the silicon layer, the electron mobility tends to the value it has in a bulk silicon inversion layer at such a temperature, $\mu_{\rm bulk}$. (ii) Then, regardless of the temperature, we have a region between $T_w = 5$ nm and $T_w = 20$ nm, where the mobility in a DGSOI inversion layer, $\mu_{\rm DGSOI}$, is higher than $\mu_{\rm bulk}$. The factor of improvement, i.e. the quotient $\frac{\mu_{\rm DGSOI}}{\mu_{\rm bulk}}$ increases as the temperature decreases. (iii) Finally, for very thin silicon layers, mobility abruptly falls for all temperatures.

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