

## Hole mobility in silicon inversion layers: Stress and surface orientation

Guangyu Sun, Yongke Sun, Toshikazu Nishida, and Scott E. Thompson  
*Department of Electrical and Computer Engineering, University of Florida, Gainesville,  
 Florida 32611, USA*

(Received 27 June 2007; accepted 20 August 2007; published online 18 October 2007)

Hole transport in the *p*-type metal-oxide-semiconductor field-effect-transistor (*p*-MOSFET) inversion layer under arbitrary stress, surface, and channel orientation is investigated by employing a six-band  $\mathbf{k}\cdot\mathbf{p}$  model and finite difference formalism. The piezoresistance coefficients are calculated and measured at stresses up to 300 MPa via wafer-bending experiments for stresses of technological importance: uniaxial and biaxial stresses on (001) and (110) surface oriented *p*-MOSFETs with  $\langle 110 \rangle$  and  $\langle 111 \rangle$  channels. With good agreement in the measured and calculated small stress piezoresistance coefficients,  $\mathbf{k}\cdot\mathbf{p}$  calculations are used to give physical insights into hole mobility enhancement at large stress ( $\sim 3$  GPa). The results show that the maximum hole mobility is similar for (001)/ $\langle 110 \rangle$ , (110)/ $\langle 110 \rangle$ , and (110)/ $\langle 111 \rangle$  *p*-MOSFETs under uniaxial stress, although the enhancement factor is different. Strong quantum confinement and a low density of states cause less stress-induced mobility enhancement for (110) *p*-MOSFETs. For (001) *p*-MOSFETs, the dominant factor for the improved hole mobility is reduced conductivity effective mass at small stress and lower phonon scattering rate at large stress. © 2007 American Institute of Physics. [DOI: 10.1063/1.2795649]

### I. INTRODUCTION

As the era of simple scaling of silicon (Si) complementary metal-oxide-semiconductor (CMOS) transistors is ending, feature-enhanced technology becomes important in order to maintain the historical performance improvement. One key feature that is utilized to improve the hole mobility in 90, 65, and 45 nm technology nodes is uniaxial compressive stress.<sup>1–6</sup> Over 200% hole mobility enhancement has been measured on (001)/ $\langle 110 \rangle$  *p*-type metal-oxide-semiconductor field-effect transistors (*p*-MOSFETs) with 2 GPa uniaxial stress.<sup>7,8</sup> Another method to improve *p*-MOSFET performance is using (110) surface which has  $\sim 100\%$  higher unstrained hole mobility.<sup>9–12</sup>

To date, emphasis has been placed on the experimental study of (001)- versus (110)- oriented *p*-MOSFETs with only a few recent theoretical results published due to the complex valence band structure of Si. In comparison to (001)/ $\langle 110 \rangle$  devices, Wang reported that, under uniaxial stress, (110)/ $\langle 111 \rangle$  *p*-MOSFETs have larger piezoresistance coefficient, while (110)/ $\langle 110 \rangle$  *p*-MOSFETs have smaller piezoresistance coefficient.<sup>12</sup> For holes in the inversion layers, the first theoretical work on strain enhanced hole mobility was reported by Oberhuber et al.<sup>13</sup> for (001)/ $\langle 110 \rangle$ Si *p*-MOSFETs under biaxial stress using self-consistent evaluation of Schrödinger and Poisson equations. Fischetti et al.<sup>14</sup> extended this work on biaxial stress to include Si thickness and surface orientation of *p*-MOSFETs. The first theoretical work of uniaxial stress on (110) surface was reported by Ouyang et al.<sup>15</sup> who shows that, with 1% uniaxial strain (about 1.6 GPa of uniaxial stress), the hole mobility enhancement is smaller in (110)/ $\langle 110 \rangle$  than (001)/ $\langle 110 \rangle$  *p*-MOSFETs. Both Refs. 14 and 15 focus on the hole mobility dependence on the

electric field rather than the stress, and triangular potential approximation was used to model the inversion layer.

The goal of this work is to provide more complete set of piezoresistance coefficients and physical insights into the uniaxial stress enhanced hole mobility in the inversion layers for (001) and (110) surface *p*-MOSFETs as a function of stress. The maximum mobility enhancement at large stress is calculated and the physics is explained via the stress-induced change of valence band and subband structures, hole effective mass, phonon, and surface roughness scattering rate.

### II. $\mathbf{k}\cdot\mathbf{p}$ METHOD, SCATTERING MECHANISM, AND MOBILITY MODEL

In this work, the  $\mathbf{k}\cdot\mathbf{p}$  method is utilized due to its simplicity and accuracy in modeling the valence band and subband properties adjacent to the  $\Gamma$  point. The  $\mathbf{k}\cdot\mathbf{p}$  method uses a small set of basis vectors and treats strained band structures with high precision.<sup>15</sup> Based on the theory of Luttinger and Kohn<sup>16</sup> and Bir and Pikus,<sup>17</sup> the bulk valence band structure of strained Si is described with a  $6\times 6$  Hamiltonian in the envelope-function space.<sup>18</sup> In the Si inversion layer, holes are confined in the quantum well that is formed by the oxide barrier and the silicon valence band, which requires a two-dimensional (2D) treatment.<sup>19</sup> To investigate the motion of the holes in the quantum well,  $k_z$  is replaced in the Luttinger-Kohn Hamiltonian with  $-i\partial/\partial z$ , assuming  $z$  is perpendicular to the Si/SiO<sub>2</sub> interface. A self-consistent solution of the coupled Schrödinger and Poisson Equation is employed to obtain the potential energy in the quantum well. The finite difference method<sup>13</sup> is utilized to evaluate both equations numerically. The subband structure in the  $k_x$ - $k_y$  plane is then obtained, and the 2D density of states (DOS) of each subband is evaluated numerically. The hole mobility is calculated using a linearization of the Boltzmann equation.<sup>14</sup>

TABLE I. Calculated and measured piezoresistance coefficients for Si *p*-MOSFETs with (001) or (110) surface orientation.

Substrate	(001)	(110)	
Channel	$\langle 110 \rangle$	$\langle 110 \rangle$	$\langle 111 \rangle$
	Measured/Calculated		
$\pi_L$	71.7 <sup>a</sup> /72.2	27.3(8.8) <sup>b</sup> /34	86 <sup>c</sup> /79.1
$\pi_T$	-33.8 <sup>a</sup> /-45.8	-5.1(3) <sup>b</sup> /-6.6	-50 <sup>c</sup> /-43
$\pi_{\text{Biaxial}}$	40 <sup>b</sup> /35.7	25.8(2.2) <sup>b</sup> /28.7	15.1 <sup>b</sup> /10.2

<sup>a</sup>Reference 32.<sup>b</sup>This work.<sup>c</sup>Reference 12.

The momentum relaxation time  $\tau$  is evaluated by considering phonon and surface roughness scattering. Charged and neutral impurity scattering is neglected since only high transverse electric field is considered (inversion charge density  $\sim 1 \times 10^{13}/\text{cm}^2$ ). The equipartition approximation<sup>20</sup> is used where the anisotropic hole-phonon matrix element is replaced with appropriate angle-averaged quantities,<sup>14,20</sup> since only high lattice temperatures ( $T=300$  K) are considered in the calculation. The detailed procedure of the scattering rate calculation can be found in Refs. 14 and 20–22.

### III. RESULTS

In this section, the hole mobility dependence on stress, surface, and channel orientation are calculated, measured, and discussed. Calculated piezoresistance coefficients are compared with experimental data obtained from four-point and concentric-ring wafer bending.<sup>5</sup> To understand the physics behind strain effects, quantum confinement and strain induced changes on subband structure and scattering rate are analyzed.

#### A. Piezoresistance coefficient

The piezoresistance coefficient ( $\pi$ ) is widely used as an effective approach for characterizing the resistance change at small stress.<sup>23,24</sup> It is defined as  $(1/\sigma)(\Delta\rho/\rho)$ , where  $\sigma$  is the applied stress and  $\rho$  is the resistance of the sample. Table I compares calculated and measured piezoresistance coefficients. The measured data are obtained on industrial samples with long channel length ( $\sim 10 \mu\text{m}$ ),  $\sim 1 \times 10^{17}/\text{cm}^3$  doping concentration,  $p^+$  poly-Si gate and 1.5 nm  $\text{SiO}_2$  gate insulator. The piezoresistance coefficients are obtained via linear regression of the measured resistance versus applied mechanical stress (0– $\sim 300$  MPa), which is achieved by four-point (uniaxial) or concentric-ring (biaxial) wafer bending. The applied mechanical stress is calculated through the resistance change of a strain gauge mounted on the samples and via laser-detected curvature change of the bent wafer. In Table I,  $\pi_L$ ,  $\pi_T$ , and  $\pi_{\text{Biaxial}}$  are the longitudinal, transverse, and in-plane biaxial piezoresistance coefficients, respectively. Both measured and calculated results show that under uniaxial longitudinal compressive stress, (110)/ $\langle 111 \rangle$  *p*-MOSFETs have the largest piezoresistance coefficient, followed by the (001)/ $\langle 110 \rangle$  *p*-MOSFETs, and the piezoresistance coefficient of (110)/ $\langle 110 \rangle$  *p*-MOSFETs is the lowest. Under uniaxial transverse tensile stress, the piezoresistance

coefficients are smaller than longitudinal stress for all *p*-MOSFETs. For both (001) and (110) surfaces, biaxial tensile stress increases the channel resistance and degrades the hole mobility at small stress. In comparison to other reported piezoresistance coefficients<sup>12</sup> where data exist, good agreement is found in both the calculated values and measured data.

#### B. Hole mobility versus surface orientation

Surface and channel orientation dependence of the electron and hole mobility has been investigated experimentally since the 1960s.<sup>25,26</sup> Sato *et al.*<sup>25</sup> reported that for *p*-MOSFETs with  $\langle 110 \rangle$  channel, the hole mobility is the highest on (110) and lowest on (001) *p*-MOSFETs. The hole mobility on various surface orientations is simulated and compared with Sato *et al.*'s experimental data in Fig. 1 where two different surface roughness scattering models (Fischetti *et al.*'s<sup>14</sup> and Gamiz *et al.*'s<sup>22</sup>) are used in the calculation. Both models have good agreement with the measured data, and Gamiz *et al.*'s model is utilized for the rest of the results.

Calculated hole mobility versus the effective electric field of unstrained (001)/ $\langle 110 \rangle$  and (110)/ $\langle 110 \rangle$  *p*-MOSFETs are compared with experimental mobility curves in Fig. 2.<sup>9,27,28</sup> The calculated results match experimental data which suggests reasonable phonon and surface

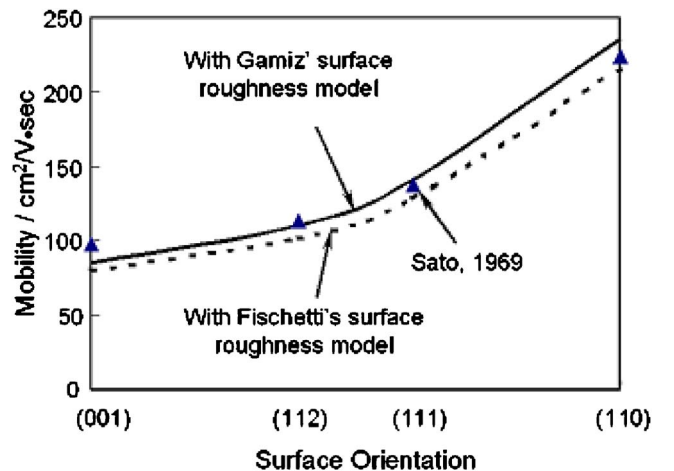


FIG. 1. (Color online) Hole mobility vs surface orientation for unstressed Si *p*-MOSFETs with  $\langle 110 \rangle$  channel. The calculation (lines) confirms that the hole mobility is the highest on (110) and lowest on (001) *p*-MOSFETs.

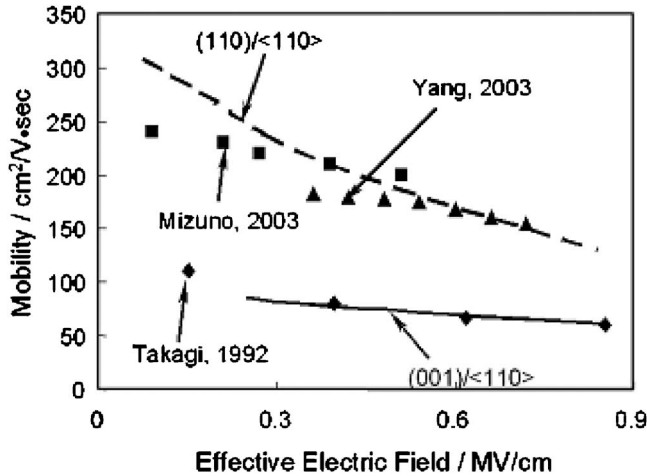


FIG. 2. Hole mobility of unstressed Si  $p$ -MOSFETs vs effective electric field in the channel. The superior mobility on (110) devices is partly due to the smoother Si/SiO<sub>2</sub> interface.

roughness scattering rates are used in this work. It has been reported that (110) Si has a smoother interface with the gate dielectric material<sup>29,30</sup> and, hence, has lower surface roughness scattering rate. Lee *et al.*<sup>31</sup> suggests that the effective electric field in (110)  $p$ -MOSFETs should also be smaller than that in (001)  $p$ -MOSFETs, which leads to reduced surface roughness scattering since the scattering rate is proportional to the effective electric field.<sup>14,22</sup> The reduced surface roughness scattering rate is partly responsible for the higher hole mobility in unstrained (110)  $p$ -MOSFETs compared to (001)  $p$ -MOSFETs. To account for the different surface roughness conditions in our calculation, the roughness parameters used for (001) and (110)  $p$ -MOSFETs are  $L=2.6$  nm,  $\Delta=0.4$  nm (Ref. 14) and  $L=1.03$  nm,  $\Delta=0.27$  nm,<sup>22</sup> respectively. We use these same surface roughness parameters for the strained Si calculation in the next sections since, unlike wafer based biaxial strain, process-induced strain is introduced after the gate insulator growth, thus it should not change the Si and gate insulator interface properties.<sup>14</sup>

### C. Strain enhanced hole mobility

Uniaxial compressive stress has been reported to have larger mobility enhancement than biaxial stress on (001)  $p$ -MOSFETs.<sup>7,8</sup> Hole mobility versus stress (longitudinal uniaxial and biaxial tensile up to 3 GPa) at inversion charge density  $p_{inv}=1 \times 10^{13}/\text{cm}^2$  is shown in Fig. 3 for (001)/<110>, (110)/<111>, and (110)/<110>  $p$ -MOSFETs. Figure 3 shows that uniaxial stress improves the hole mobility monotonically as the stress increases for all cases, while biaxial stress on (001)/<110>  $p$ -MOSFETs degrades the hole mobility at small stress and enhances the hole mobility at large stress. As the stress increases to  $\sim 3$  GPa, the enhancement of the hole mobility saturates. The maximum hole mobility enhancement factor is about  $\sim 100\%$  under biaxial stress. Under uniaxial stress, the enhancement is 350% for (001)/<110>  $p$ -MOSFETs,  $\sim 150\%$  for (110)/<111>  $p$ -MOSFETs, and  $\sim 100\%$  for (110)/<110>  $p$ -MOSFETs. Under 3 GPa uniaxial stress, (001) and (110)  $p$ -MOSFETs have

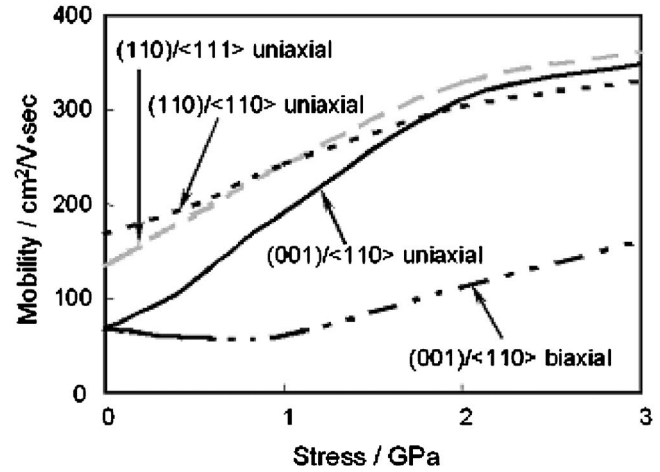


FIG. 3. Hole mobility vs stress (inversion charge= $1 \times 10^{13}/\text{cm}^2$ ). The enhancement factor is the highest for (001)/<110> and lowest for (110)/<110>  $p$ -MOSFETs. At high stress ( $\sim 3$  GPa), the three longitudinal compressive uniaxial stress cases have comparable hole mobility.

comparable hole mobility, although the enhancement factor for both (110)/<110> and (110)/<111>  $p$ -MOSFETs is smaller than (001)/<110>  $p$ -MOSFETs.

### D. Strain altered subband structure

To understand the measured and calculated strain enhanced hole mobilities, we start with the strain altered band structure since the hole effective mass change is a dominant factor, especially at small stress.<sup>32</sup> Strain lifts the degeneracy of the heavy-hole (HH) and light-hole (LH) bands at the  $\Gamma$  point and alters the curvature of both bands. Detailed discussion of the strain induced change in the hole effective mass and the energy contours can be found in Refs. 5 and 32. In general, the property of each band under strain has a strong dependence on crystal orientation. A single band may be HH-like along one direction while LH-like along the other.<sup>33</sup> Since HH and LH bands lose their meanings under strain, the topmost two valence bands are referred to as “top band” and “second band” in this work according to their energy at  $\Gamma$  point. For a generic strain, the top band is HH-like along the direction of tensile strain and LH-like along the direction of compressive strain.<sup>33</sup> For uniaxial longitudinal compressive stress on (001)/<110>  $p$ -MOSFETs, the top band is LH-like along <110> (compression) and HH-like out of plane (tension). For biaxial tensile stress on (001)  $p$ -MOSFETs, the top band is HH-like in plane and LH-like along the out-of-plane direction. Thus, the top band effective mass along the <110> direction is smaller under uniaxial compressive stress than biaxial tensile stress ( $0.12m_0$  vs  $0.29m_0$ ).<sup>5,19</sup>

In  $p$ -MOSFETs, the topmost two subbands, the top (ground state) and the second (first excited state) subbands, contain most of the holes. Hence, analyzing those two subbands gives us qualitative understanding of the hole transport properties. These two subbands will be considered in the following discussion to explain the strain effects, although up to 30 subbands are actually taken into account in the mobility calculation. For longitudinal uniaxial compression on (110), similar to (001)/<110>  $p$ -MOSFETs, the top sub-

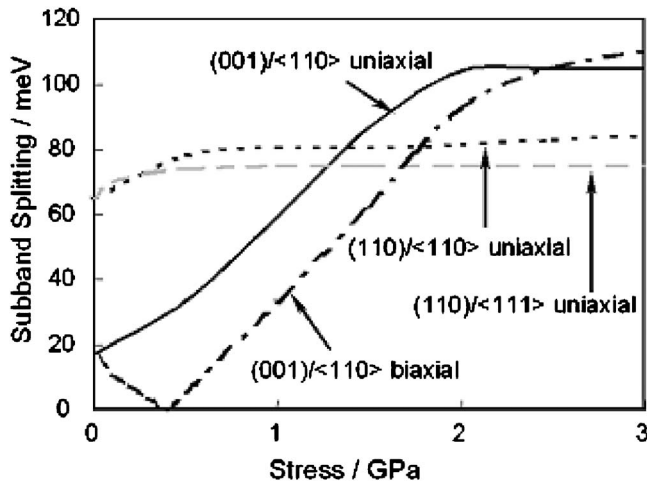


FIG. 4. Energy splitting between the top and second subband vs stress ( $E_{\text{eff}}=0.6$  MV/cm). In (110)  $p$ -MOSFETs, the splitting increases little at large stress ( $> \sim 1$  GPa).

band of both  $\langle 110 \rangle$  and  $\langle 111 \rangle$   $p$ -MOSFETs is LH-like along the channel and HH-like in the out-of-plane direction. However, the out-of-plane effective mass of the top subband of (110) is much larger,<sup>32</sup> which results in greater subband splitting at small stress, as shown in Fig. 4. The subband splitting of (110) Si is mainly caused by the strong quantum confinement and has weak dependence on the applied stress, which is opposite to (001)  $p$ -MOSFETs.

To understand the difference of confinement effects on (001) and (110)  $p$ -MOSFETs, confined 2D energy contours (25, 50, 75, and 100 meV) of the top subband are shown in Fig. 5. For (001)/ $\langle 110 \rangle$   $p$ -MOSFETs under uniaxial compressive stress, the conductivity effective mass of holes in the top subband decreases as the stress increases [Fig. 5(a)]. The effective mass change under biaxial stress is not that significant<sup>5</sup> [Fig. 5(b)]. Compared with the bulk Si energy contours in Refs. 5 and 32, the electric field causes little change of the subband structure in  $k_x$ - $k_y$  plane for (001)  $p$ -MOSFETs resulting in the conductivity effective masses along the channel direction almost identical to the bulk Si effective masses. For (110)  $p$ -MOSFETs, the quantum con-

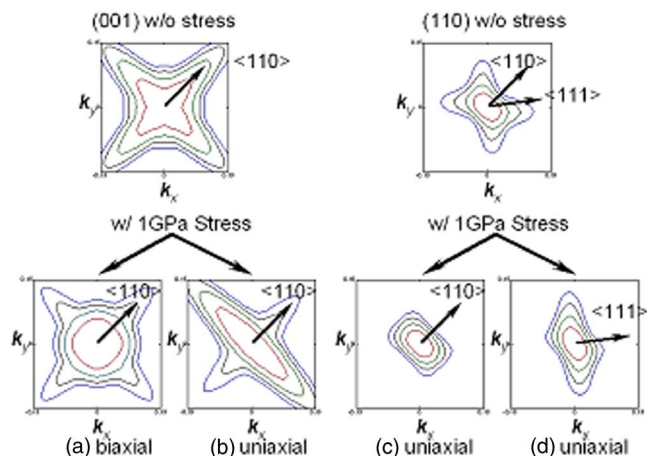


FIG. 5. (Color online) Confined 2D energy contours. As seen from the stress altered contours, the effective mass along channel direction decreases the most for (b) and (d) and leads to the highest mobility enhancement.

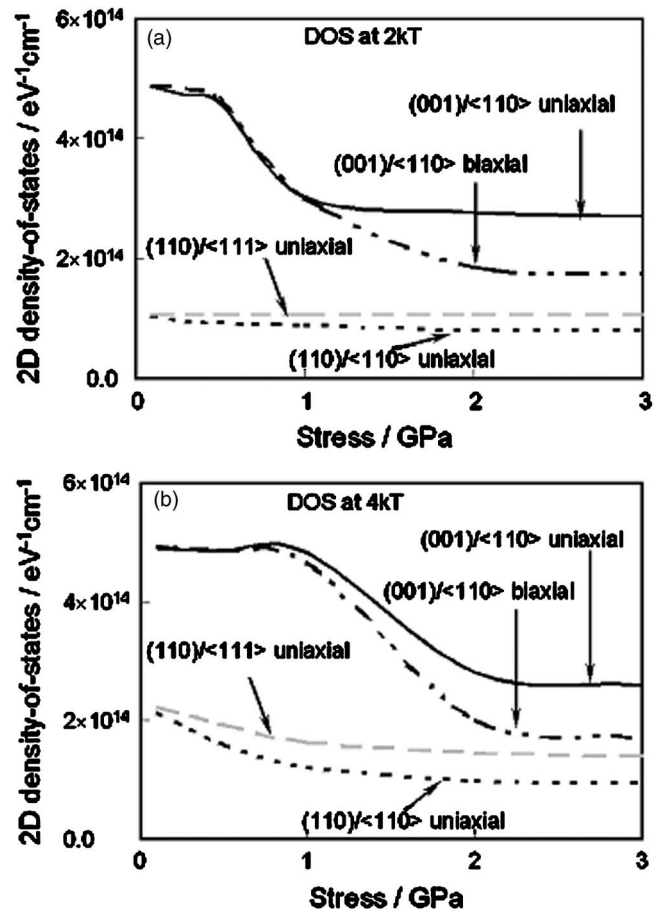


FIG. 6. DOS vs stress for the top subband at (a) energy= $2kT$  and (b) energy= $4kT$ . In (001)  $p$ -MOSFETs, DOS decreases as the stress increases. In (110)  $p$ -MOSFETs, strong quantum confinement results in smaller stress-induced DOS change.

finement causes drastic change of the subband structures compared with their bulk counterparts.<sup>12</sup> It leads to low conductivity effective mass along  $\langle 110 \rangle$  and  $\langle 111 \rangle$  directions in unstrained (110)  $p$ -MOSFETs, which results in higher unstrained hole mobility than (001)  $p$ -MOSFETs. As the stress increases, the regions close to  $\Gamma$  point [see inner rings, Figs. 5(c) and 5(d)] in each subband are not warped as much as the regions away from  $\Gamma$  point [see outer rings, Figs. 5(c) and 5(d)]. This suggests that the average hole effective mass change is small since most holes locate at low energy region in each subband. This small change in average effective mass leads to smaller mass-induced mobility change for (110) than (001)  $p$ -MOSFETs. The warping of the contours in Figs. 5(c) and 5(d) also suggests that hole effective mass decrease more in (110)/ $\langle 111 \rangle$  than (110)/ $\langle 110 \rangle$   $p$ -MOSFETs.

The strain altered 2D DOS also changes the phonon scattering rate. The different strain effect in (001) and (110)  $p$ -MOSFETs can be seen from the 2D DOS change in Fig. 6, where DOSs at energies of  $\sim 2kT$  (52 meV at  $T=300$  K) and  $\sim 4kT$  (104 meV at  $T=300$  K) are shown. Stress-induced DOS change in (001) Si suggests that the band/subband structure is not warped uniformly by the stress in  $\mathbf{k}$  space. The band warping starts from  $\Gamma$  point under small stress. As the stress increases, more regions in each band are warped. The barely changed DOS of (001)  $p$ -MOSFETs at small

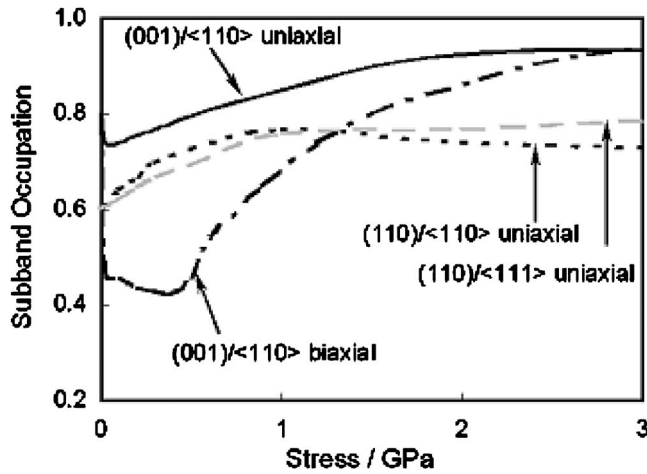


FIG. 7. Top subband occupation vs stress. For (110) *p*-MOSFETs under large stress (1–3 GPa), the small change in hole population leads to little intersubband phonon scattering reduction and small mobility enhancement.

stress ( $\sim < 500$  MPa) in Fig. 6(a) suggests that at this energy ( $\sim 2kT$ ), the subband structure is not distorted much by the stress. As the stress increases above  $\sim 500$  MPa, the subband at energy  $\sim 2kT$  is warped severely by the stress causing the decrease of the DOS. At even larger stress, the DOS does not change with stress due to the saturation of the subband warping. Figures 6(a) and 6(b) also shows that stress does not significantly alter the DOS in (110) *p*-MOSFETs.

The DOS and the subband splitting determine the population of holes in the top subband. A large population of holes in a top subband with a small conductivity effective mass in the channel direction is desired for high mobility. Figure 7 plots the hole population of the top subband under stress. For (001) *p*-MOSFETs, the hole population is large since the top subband has large DOS. As the uniaxial stress increases, the average hole conductivity effective mass decreases since holes in the top subband become LH-like along the  $\langle 110 \rangle$  direction. The hole population in the top subband also increases due to the increasing subband splitting, as shown in Fig. 4. In Fig. 7, we also observe for biaxial stress, a decreasing hole population at small stress due to the reduced subband splitting. For (110) *p*-MOSFETs, the top subband hole population is smaller than (001) *p*-MOSFETs and increases less as the stress increases, which results from the relative constant subband splitting, in Fig. 4 and the low 2D DOS, as shown in Fig. 6.

### E. Stress-reduced hole scattering rate

Stress-induced hole scattering reduction is an important factor to enhance hole mobility, though there is uncertainty in the benefit to nanoscale MOSFETs.<sup>34,35</sup> Phonon and surface roughness scattering rates versus stress in Si inversion layers are shown in Figs. 8 and 9. The results show that optical phonon scattering is dominant among the three scattering mechanisms.

In (001) *p*-MOSFETs, the phonon scattering rate is approximately constant for stress less than  $\sim 500$  MPa, as seen in Figs. 8(a) and 8(b). Thus at small stress, the effective mass change is primarily responsible for the enhanced hole mobil-

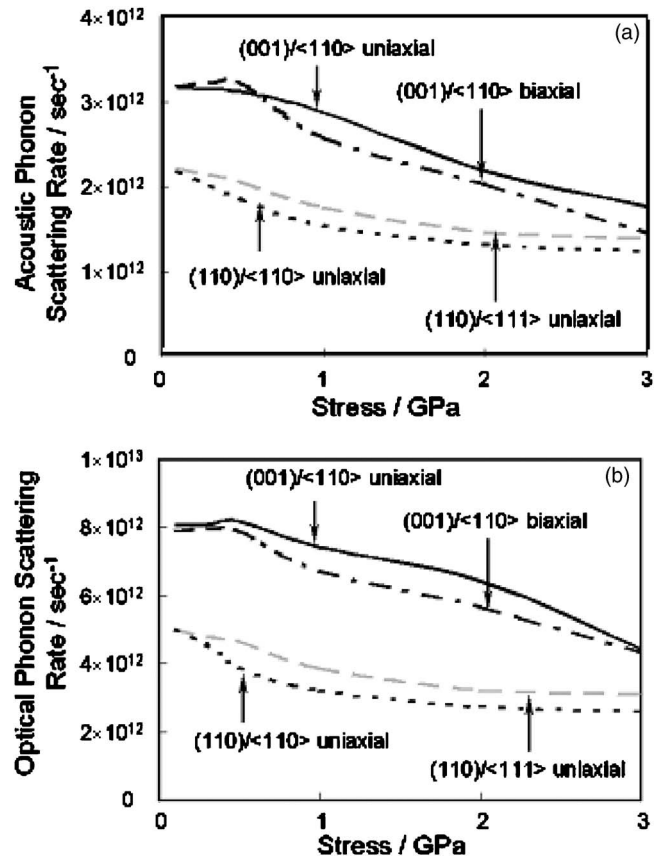


FIG. 8. (a) Acoustic and (b) optical phonon scattering rates vs stress. The decrease in optical phonon scattering is dominant to improve the hole mobility as the stress increases. Phonon scattering rate reduces mainly in large stress region for (001) and small stress region for (110) *p*-MOSFETs.

ity. As the stress increases from  $\sim 500$  MPa to 3 GPa, the phonon scattering rate decreases by 50% and enhances mobility. The phonon scattering rate decreases due to the increased subband splitting (see Fig. 4) and the decreased 2D DOS (see Fig. 6). Compared with (001) Si, the phonon scattering rate in (110) *p*-MOSFETs decreases less mainly because of a smaller change in the 2D DOS (see Fig. 6). Another difference is that the scattering rate change is mainly at

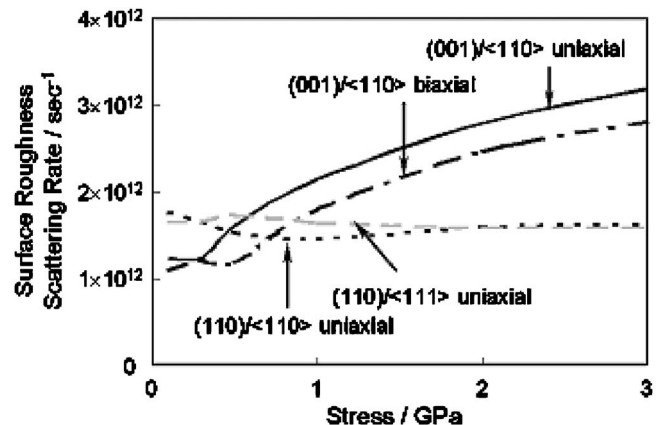


FIG. 9. Surface roughness scattering rate vs stress. As stress increases, the scattering rate increases in (001) *p*-MOSFETs due to the increasing occupation in the top subband resulting in the hole centroids closer to the Si/SiO<sub>2</sub> interface. In (110) *p*-MOSFETs, the scattering rate is approximately constant because of the little change of the hole repopulation.

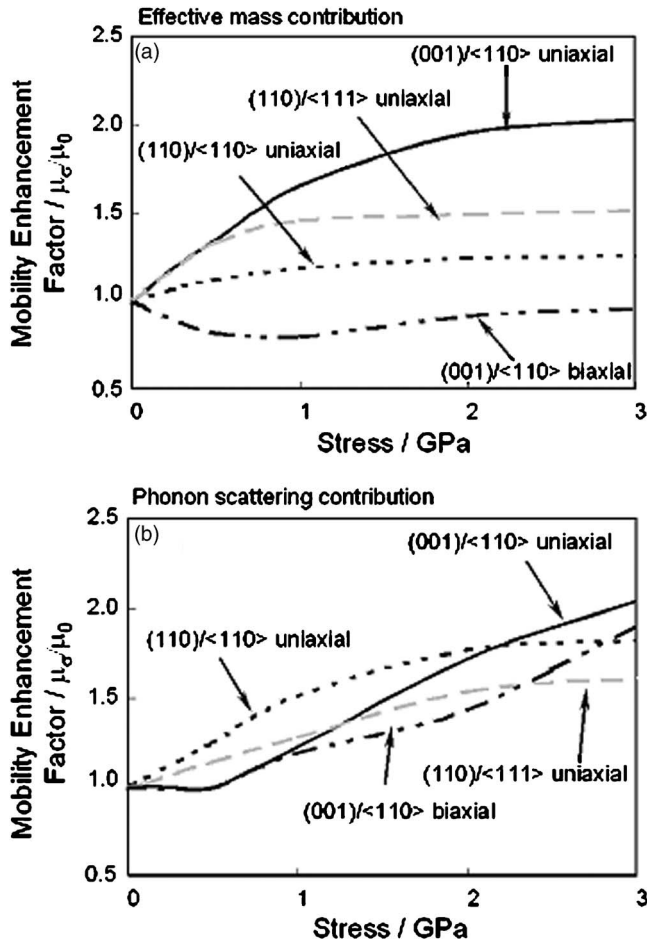


FIG. 10. Mobility enhancement due to (a) effective mass change and (b) phonon scattering rate change. Uniaxial stress on (001)/<110> *p*-MOSFETs causes the largest enhancement in both cases.

small stress. This is consistent with Figs. 4 and 7 that the subband splitting and the top subband hole population only increase at small stress for (110) *p*-MOSFETs.

Stress altered surface roughness scattering is also different for (001) and (110) *p*-MOSFETs. Figure 9 shows that, for (001) *p*-MOSFETs, surface roughness scattering rate increases with stress because the increasing hole occupation in the top subband leads to the hole centroid closer to the Si/SiO<sub>2</sub> interface. Stress induces little change of the surface roughness scattering rate for (110) *p*-MOSFETs because the top subband hole population is relatively constant versus stress.

The mobility enhancement due to reduced effective mass and phonon scattering is shown in Figs. 10(a) and 10(b), respectively. Under uniaxial stress, (001)/<110> *p*-MOSFETs have the largest mobility enhancement from both the effective mass and scattering rate changes. Biaxial tensile stress slightly increases the effective mass. For (110)/<110> versus (001)/<110> *p*-MOSFETs, the effective mass gain is significantly smaller but the phonon scattering gain is comparable. In (110)/<111> *p*-MOSFETs, the lack of gain from both effective mass and phonon scattering at large stress (> ~1.5 GPa) explains why the hole mobility at 3 GPa is not significantly larger than (001)/<110> or (110)/<110> *p*-MOSFETs, regardless of the largest piezoresistance coef-

ficient at small stress. Compared with (110)/<110> *p*-MOSFETs, (110)/<111> *p*-MOSFETs have higher mobility gain from the reduced effective mass but smaller mobility gain from the decrease of the phonon scattering rate.

#### IV. CONCLUSION

Piezoresistance coefficients are measured and the physics of longitudinal uniaxial stress enhanced hole mobility is explained for (001) and (110) *p*-MOSFETs. Calculation shows that low conductivity effective mass, high DOS of the top subband, and small intersubband phonon scattering are all critical to large hole mobility enhancement in (001) *p*-MOSFETs with stress. The strong quantum confinement in (110) *p*-MOSFETs leads to smaller change in effective mass and phonon scattering rate, which results in less hole mobility improvement. The physics introduced in this work also applies to thin channel devices, i.e., silicon-on-insulator (SOI) and double-gate (DG) *p*-MOSFETs, providing the potential profile in the channel is similar to the bulk case. For channel thickness less than ~10 nm, subband splitting in SOI (planar, DG, or Fin-shaped field-effect-transistor (FinFETs)) under stress will be different due to the structural confinement and subband modulation.<sup>36</sup> For this case, the stress-induced hole mobility change should be different, but it has not been observed experimentally.<sup>37-39</sup>

#### ACKNOWLEDGMENTS

The authors would like to thank the Applied Materials Foundation, Advanced Micro Devices (AMD), Cypress Semiconductor, IBM, Intel Foundation, Semiconductor Research Corporation (SRC), Texas Instruments, Taiwan Semiconductor Manufacturing Company (TSMC), Multidisciplinary University Research Initiative (MURI), and the National Science Foundation (NSF) under Grant No. ECS-0524316 for funding this research.

<sup>1</sup>T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. McIntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson, and M. Bohr, Tech. Dig. - Int. Electron Devices Meet. **2003**, 1161.

<sup>2</sup>V. Chan, R. Rengarajan, N. Rovedo, W. Jin, T. Hook, P. Nguyen, J. Chen, E. Nowak, X.-D. Chen, D. Lea, A. Chakravarti, V. Ku, S. Yang, A. Steegen, C. Baiocco, P. Shafer, H. Ng, S.-F. Huang, and C. Wann, Tech. Dig. - Int. Electron Devices Meet. **2003**, 381.

<sup>3</sup>C. Chien-Hao, T. L. Lee, T. H. Hou, C. L. Chen, C. C. Chen, J. W. Hsu, K. L. Cheng, Y. H. Chiu, J. J. Tao, Y. Jin, C. H. Diaz, S. C. Chen, and M. S. Liang, Tech. Dig. VLSI Symp. **2004**, 56.

<sup>4</sup>Y. C. Liu, J. W. Pan, T. Y. Chang, P. W. Liu, B. C. Lan, C. H. Tung, C. H. Tsai, T. F. Chen, C. J. Lee, W. M. Wang, Y. A. Chen, H. L. Shih, L. Y. Tung, L. W. Cheng, T. M. Shen, S. C. Chiang, M. F. Lu, W. T. Chang, Y. H. Luo, D. Nayak, D. Gitlin, H. L. Meng, and C. T. Tsai, Tech. Dig. - Int. Electron Devices Meet. **2005**, 836.

<sup>5</sup>S. E. Thompson, G. Sun, K. Wu, J. Lim, and T. Nishida, Tech. Dig. - Int. Electron Devices Meet. **2004**, 221.

<sup>6</sup>S. E. Thompson, M. Armstrong, C. Auth, S. Cea, R. Chau, G. Glass, T. Hoffman, J. Klaus, Z. Ma, B. McIntyre, A. Murthy, B. Obradovic, L. Shifren, S. Sivakumar, S. Tyagi, T. Ghani, K. Mistry, M. Bohr, and Y. El-Mansy, IEEE Electron Device Lett. **25**, 191 (2004).

<sup>7</sup>L. Smith, V. Moroz, G. Eneman, P. Verheyen, F. Nouri, L. Washington, M. Jurczak, O. Penzin, D. Pramanik, and K. D. Meyer, IEEE Electron Device Lett. **26**, 652 (2005).

<sup>8</sup>L. Washington, F. Nouri, S. Thirupapuliur, G. Eneman, P. Verheyen, V. Moroz, L. Smith, X. Xu, M. Kawaguchi, T. Huang, K. Ahmed, M.

- Balseanu, Li-Qun Xia, M. Shen, Y. Kim, R. Roovachers, K. D. Meyer, and R. Schreutelkamp, *IEEE Electron Device Lett.* **27**, 511 (2006).
- <sup>9</sup>M. Yang, M. Jeong, L. Shi, K. Chan, V. Chan, A. Chou, E. Gusev, K. Jenkins, D. Boyd, Y. Ninomiya, D. Pendleton, Y. Supris, D. Heenan, J. Ott, K. Guarini, C. D'Emic, M. Cobb, P. Mooney, B. To, N. Rovedo, J. Benedict, R. Mo, and H. Ng, *Tech. Dig. - Int. Electron Devices Meet.* **2003**, 453.
- <sup>10</sup>M. Yang, E. Gusev, M. Jeong, O. Gluschenkov, D. Boyd, K. Chan, P. Kozlowski, C. D'Emic, R. Sicina, P. Jamison, and A. Chou, *IEEE Electron Device Lett.* **24**, 339 (2003).
- <sup>11</sup>T. Mizuno, N. Sugiyama, T. Tezuka, Y. Moriyama, S. Nakaharai, and S. Takagi, *IEEE Trans. Electron Devices* **52**, 367 (2005).
- <sup>12</sup>H. Wang, S. Huang, C. Tsai, H. Lin, T. Lee, S. Chen, C. Diaz, M. Liang, and J. Sun, *Tech. Dig. - Int. Electron Devices Meet.* **2006**, 309.
- <sup>13</sup>R. Oberhuber, G. Zandler, and P. Vogl, *Phys. Rev. B* **58**, 9941 (1998).
- <sup>14</sup>M. V. Fischetti, Z. Ren, P. M. Solomon, M. Yang, and K. Rim, *J. Appl. Phys.* **94**, 1079 (2003).
- <sup>15</sup>Q. Ouyang, M. Yang, J. Holt, S. Panda, H. Chen, H. Utomo, M. Fischetti, N. Rovedo, J. Li, N. Klymko, H. Wildman, T. Kanarsky, G. Costrini, D. M. Fried, A. Bryant, J. A. Ott, M. Jeong, and C. Sung, *Tech. Dig. VLSI Symp.* **2005**, 28.
- <sup>16</sup>J. M. Luttinger and M. Kohn, *Phys. Rev.* **97**, 869 (1955).
- <sup>17</sup>G. L. Bir and G. E. Pikus, *Symmetry and Strain-Induced Effects in Semiconductors* (Wiley, New York, 1974).
- <sup>18</sup>C. Chao and S. L. Chuang, *Phys. Rev. B* **46**, 4110 (1992).
- <sup>19</sup>Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices* (Cambridge University Press, Cambridge, 1998), Chap. 4, p. 194.
- <sup>20</sup>B. K. Ridley, *Quantum Processes in Semiconductors* (Oxford Science, Oxford, 1999).
- <sup>21</sup>K. Matsuda, H. Nakatsuji, and Y. Kamakura, *Tech. Proc. Nanotech. Conf. and Trade Show*, 186 (2003).
- <sup>22</sup>F. Gamiz, J. B. Roldan, J. A. Lopez-Villanueva, P. Cartujo-Cassinello, and J. E. Carceller, *J. Appl. Phys.* **86**, 6854 (1999).
- <sup>23</sup>C. S. Smith, *Phys. Rev.* **94**, 42 (1954).
- <sup>24</sup>D. Colman, R. T. Bate, and J. P. Mize, *J. Appl. Phys.* **39**, 1923 (1968).
- <sup>25</sup>T. Sato, Y. Takeishi, and H. Hara, *Jpn. J. Appl. Phys.* **8**, 588 (1969).
- <sup>26</sup>T. Sato, Y. Takeishi, and H. Hara, *Phys. Rev. B* **4**, 1950 (1971).
- <sup>27</sup>S. Takagi, A. Toriumi, M. Iwase, and H. Tango, *IEEE Trans. Electron Devices* **41**, 2363 (1994).
- <sup>28</sup>T. Mizuno, N. Sugiyama, T. Tezuka, Y. Moriyama, S. Nakaharai, T. Maeda, S. Takagi, *Tech. Dig. - Int. Electron Devices Meet.* **2003**, 809.
- <sup>29</sup>M. M. Chowdhury and J. G. Fossum, *IEEE Electron Device Lett.* **27**, 482 (2006).
- <sup>30</sup>M. L. Green, D. Brasen, K. W. Evans-Lutterodt, L. C. Feldman, K. Krisch, W. Lennard, H. Tang, and L. Manchanda, *Appl. Phys. Lett.* **65**, 848 (1994).
- <sup>31</sup>K. Lee, J. Choi, S. Sim, and C. Kim, *IEEE Trans. Electron Devices* **38**, 1905 (1991).
- <sup>32</sup>S. E. Thompson, G. Sun, Y. Choi, and T. Nishida, *J. Appl. Phys.* **53**, 1010 (2006).
- <sup>33</sup>Y. Sun, S. E. Thompson, and T. Nishida, *J. Appl. Phys.* **101**, 104503 (2007).
- <sup>34</sup>M. Lundstrom and Z. Ren, *IEEE Trans. Electron Devices* **49**, 133 (2002).
- <sup>35</sup>O. Weber and S. Takagi, *Tech. Dig. VLSI Symp.* **2007**, 130.
- <sup>36</sup>V. P. Trivedi, J. G. Fossum, and F. Gamiz, *Tech. Dig. - Int. Electron Devices Meet.* **2004**, 763.
- <sup>37</sup>K. Shin, W. Xiong, C. Cho, C. Cleavelin, T. Schulz, K. Schrufer, P. Patruno, L. Smith, and Tsu-Jae King Liu, *IEEE Electron Device Lett.* **27**, 671 (2006).
- <sup>38</sup>N. Collaert, A. De Keersgieter, K. G. Anil, R. Rooyackers, G. Eneman, M. Goodwin, B. Eyckens, E. Sleenckx, J.-F. de Marneffe, K. De Meyer, P. Absil, M. Jurczak, and S. Biesemans, *IEEE Electron Device Lett.* **26**, 820 (2005).
- <sup>39</sup>N. Collaert, R. Rooyackers, A. De Keersgieter, F. E. Leys, I. Cayrefourcq, B. Ghyselen, R. Loo, M. Jurczak, and S. Biesemans, *IEEE Electron Device Lett.* **28**, 646 (2007).

Journal of Applied Physics is copyrighted by the American Institute of Physics (AIP).  
Redistribution of journal material is subject to the AIP online journal license and/or AIP  
copyright. For more information, see <http://ojps.aip.org/japo/japcr/jsp>