ԵՐԵՎԱՆԻ ՊԵՏԱԿԱՆ ՀԱՄԱԼՍԱՐԱՆ

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ԵՐԵՎԱՆ, 11-13 ՍԵՊՏԵՄԲԵՐԻ

SEMICONDUCTOR MICRO- AND NANOELECTRONICS

PROCEEDINGS OF THE TENTH INTERNATIONAL CONFERENCE
YEREVAN, ARMENIA, SEPTEMBER 11-13

ԵՐԵՎԱՆ 2015 YEREVAN

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Տպագրվում է Երևանի պետական համալսարանի ռադիոֆիզիկայի ֆակուլտետի գիտական խորհրդի որոշմամբ:

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Կ 510 ԳԻՏԱԺՈՂՈՎԻ ՆՅՈՒԹԵՐ ԵՐԵՎԱՆ, 11-13 ՍԵՊՏԵՄԲԵՐԻ.- Եր.: ԵՊՀ հրատ., 2015.- 180 էջ:

Ժողովածուի մեջ զետեղված են 2015 թ. սեպտեմբերի 11-13-ը Երևանում անցկացված «Կիսահաղորդչային միկրո- և նանոէլեկտրոնիկա» գիտաժողովում զեկուցված նյութերը: Աշխատանքները խմբավորված են ըստ հետևյալ բաժինների.

1. Նոր նյութեր և սարքեր,
2. Գազային և կենսաքիմիական սենսորներ
2. Նանոգիտություն և ցածր չափայնության համակարգեր,
3. Ինտեգրալ սխեմաների մշակում և մոդելավորում:

Ժողովածուն տպագրության է պատրաստվել փորձագիտական և խմբագրական հանձնախմբի կողմից:

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Armenian scientists carry out intensive investigations in the field of physics and technology of semiconductors, semiconductor devices and nanotechnologies. New important results are obtained in micro- and nano-electronics. Many reports of Armenian scientists made in co-authorship with colleagues from several countries. Important results were obtained in Armenia in process of investigations of phenomena in sensors, photocells, transistors, large ICs, low-dimensional size effects, low-frequency noises peculiarities, and noise spectroscopy etc. It is evident that the geography of our Conference is expanded.

We hope that the Conference will go in a propitious and pleasant atmosphere, where new scientific ideas and foundations for novel projects.

The Organizing Committee whishes the participant's useful work, fruitful discussions, interesting polemics, genesis of new ideas and conceptions!

Thanks to State Committee of Sciences (of Ministry of Education and Science of the Republic of Armenia), "Barva" Innovation Center for the financial support and "Synopsys Armenia CJSC" for the contribution for awarding young scientists.

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NEW MATERIALS & DEVICES

SELECTIVE NANOCHEMISTRY ON GRAPHENE/SILICON CARBIDE USING HYDROGEN/DEUTÉRIUM: NANOTUNNELS OPENING AND POLYCYCLIC AROMATIC HYDROCARBONS FORMATION

P. Soukiassian

Commissariat à l'Energie Atomiqueet aux Energies Alternatives, CEA-Saclay, 91191 Gif sur Yvette, and Synchrotron SOLEIL, Saint Aubin, 91192 Gif sur Yvette, France

Graphene & silicon carbide (SiC) are advanced semiconductors having figures of merit scaling well above those of well-established ones [1,2]. Understanding/mediating the properties of SiC and graphene surfaces &interfaces are of central importance toward functionalization & applications. As a 2D material, grapheneis a single atomic layer of carbon atoms in a *sp2* bonding configuration. Therefore, functionalization remains challenging since interacting too strongly with the graphene atomic layer may change its bonding configuration and properties. Instead, interacting with the SiC substrate offers an alternative approach. The 1st case of hydrogen-induced metallization of a semiconductor surface has been shown for a 3C-SiC(001) surface [3]. Here, combining investigations using advanced experimental techniques such as STM/STS, vibrational infrared and high resolution electron energy losses spectroscopies &3rd generation synchrotron radiation-based photoelectron(SR-PES) spectroscopy together with state-of-art *ab-initio* VASP calculations using the MedeA® environment are presented and discussed. It includes the 1st evidence of H/D-induced nanotunnel opening at a semiconductor subsurface shown here for SiC [4] – Fig. 1. Depending on H coverage, these nanotunnels could either be metallic or semiconducting – Fig. 2. The measured and computed vibrational frequencies are in excellent agreement – see Table 1. Dangling bonds generated inside the nanotunnel offer a promising template to capture atoms or molecules. These features open nanotailoring capabilities towards advanced applications in electronics, chemistry, storage, sensors or biotechnology. Understanding/controlling such a mechanism open routes towards selective surface/interface functionalization of epitaxial graphene [4].

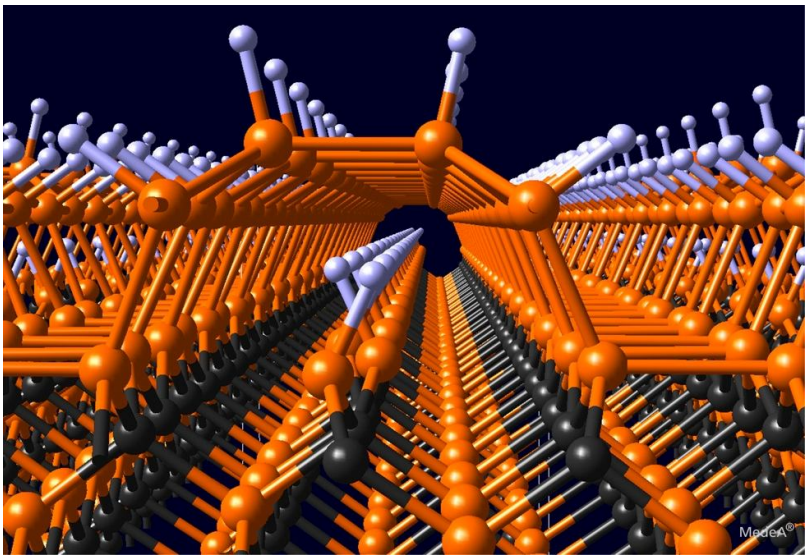

Fig. 1. Computed view of a 3D nanotunnel. The nanotunnel opening induced by the interaction of H-atoms with the 3C-SiC(100)-3x2 surface is represented for the metallic structure [4]. Note that, in the nanotunnel, the dangling bonds not terminated by a hydrogen/deuterium atom are not shown.

Hydrogen, deuterium, silicon and carbon are among the most abundant species in the universe. Silicon carbide (as SiC stardust) is also abundant in the interstellar medium resulting from the interaction between Si and C atoms at high temperatures. Indeed, at the end of the 19th century, Henri Moissan, a French scientist, discovered SiC grains on a meteorite fallen in the Diablo Canyon, Arizona [5].Polycyclic aromatic hydrocarbons (PAH) as well as other organic molecules also appear among the most abundant observed species in interstellar space and are key molecules to understanding the prebiotic roots of life. So far, however, their existence and abundance in space remain a puzzle. Here, we present a new top-down route to form polycyclic aromatic hydrocarbons in large quantities in space. We show that aromatic species can be efficiently

formed on the graphitized surface of the abundant silicon carbide stardust upon exposure to atomic hydrogen at pressure and temperature conditions analogous to those of the interstellar medium.

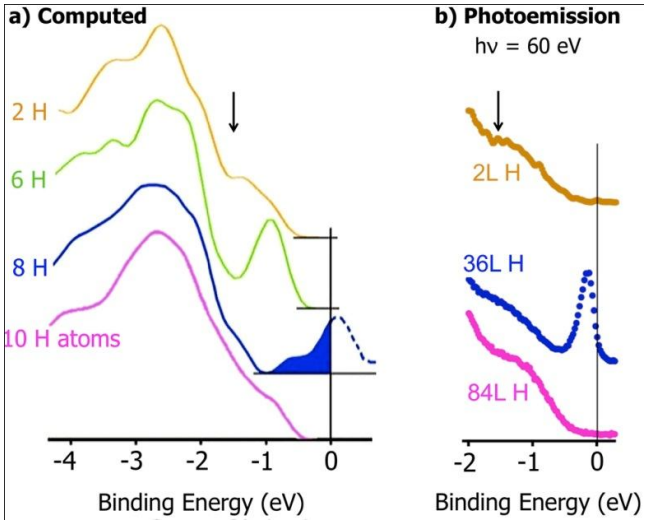

Fig. 2. SR-PES and computed DOS for H-covered 3C-SiC(001)-3x2 surfaces. (a) Computed density of states (DOS) for the 2 H, 6 H, 8 H atom and 10 H atom structures integrated over the top three Si layers and the first C layer – See Fig. 2. (b) SR-PES spectra recorded at photon energy of hn¼60 eV in the Fermi level region for 2L H exposure (semiconducting), 36L H exposure (metallic) and 84L H exposure (semiconducting) surfaces. Note the metallic–semiconducting transition upon higher H exposures in agreement with the calculated densities of states. Arrows denote the position of the surface state for the clean SiC surface, which is quenched upon H adsorption. Here also, we can note the remarkable agreement between experimentally measured DOS and computed ones [4].

Table 1 | Measured and computed vibrational frequencies of the metallic structure.

Hydrogen				Deuterium			
Theory (cm^{-1})	Infrared (cm^{-1})[23]	HREELS in specular (cm^{-1})	HREELS out of specular (cm^{-1})	Theory (cm^{-1})	HREELS in specular (cm^{-1})	HREELS out of specular (cm^{-1})	Motion occurring in the vibrational mode
600		635	600	438	Not observed	435	Wagging Si(2a)
621				422			Wagging Si(1a)
2,120	2,140			1,530			Stretch Si(3a)-H(D)
2,093	2,118			1,511			
(2,115)		2,130		(1,527)	1,540		Stretch Si(1a)-H(D)
2,087				1,506			Stretch Si(1a)—H(D)
(2,110)			2,120	(1,523)		1,532	antiphase
2,020		Not observed		1,457	Not observed		Stretch Si(2a)—H(D) in plane

Table 1. The vibrational frequencies measured (50L H(D)-exposed) and computed (8 H(D)) for the metallic structure are shown above. Frequencies are in cm^{-1}. The modes are strongly coupled. The HREELS data (50L H/D) recorded out of specular are sensitive also to the antiphase motion of the H(D) atoms bonded to first and third Si layer, while only the symmetric modes can be excited in-specular.The computed values in parentheses for the Si(1a)–H(D) stretch mode are for a structure with H(D) atoms bonding only to Si1a atoms of the surface dimer [4].

In these views, we mimic the circumstellar environment using ultra-high vacuum chambers to perform advanced experimental techniques such as STM and SR-based core-level photoemission spectroscopy (SR-CL-PES) to investigate H exposures of graphene-terminated SiC surfaces, combined with first-principles density functional theory (DFT) molecular dynamics (MD) calculations. The results suggest that top-down routesare crucial to astrochemistry to explain the abundance of organic species and to uncover the origin of unidentified infrared emission features from advanced observations. Finally, the role of H interaction with graphene on SiC dust grains in the formation of PAH is consistent with the laboratory results obtained “on earth”, showing a possible route toward prebiotic roots of life in the universe – see in Fig. 3,a qualitative scenario of such a sequence [6].

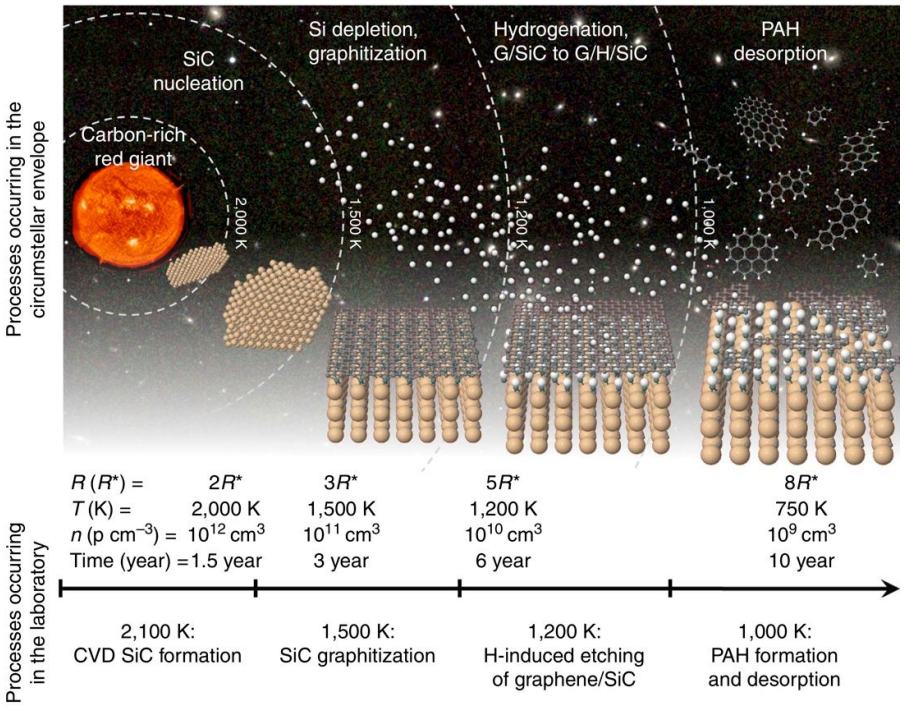

Fig. 3. Qualitative sketch of the proposed process. The steps for the formation of interstellar PAHs and aromatic-aliphatic molecules in the envelope of an evolved star can be divided into four different stages. 1) Formation of SiC in the gas phase and condensation into micrometer- and nanometer-sized grains (T=2,000 K; 1–5 R*). 2) Annealing of the SiC dust grains due to the proximity of the star and the consequent promotion of surface C-rich phases and graphene (T=2,000–1,500 K, 1–5 R*). (3) Exposures of the surface to atomic hydrogen, promoting graphitization of the C-rich surface and H passivation of the underlying buffer layer (T=1,500–1,200 K; 5–20 R*). (4) Etching of the graphene by atomic hydrogen and thermally assisted desorption of PAHs (T=1,200–1,000 K, 5–20 R*). The lower row shows the typical temperatures used in the laboratory experiments [5]. The background images used here are from NASA.

Acknowledgements

The investigations on H-induced nanotunnels opening at the SiC sub-surface have been supported in part by the EU-RU.NET European Pilot Project, by Compagnia San Paolo and by the French Agence Nationale de la Recherche through the ANR-P2 Nano MetroGraph Project. P.S. acknowledges the support of the Consiglio Nazionaledelle Ricerche (CNR) under the short-term mobility program. The authors are especially grateful to the SOLEIL staff for outstanding assistance in synchrotron radiation experiments, and to Marcin Zielinski and Thierry Chassagne from Nova SiC SARL (Sophia-Antipolis, France) and Lea di Cioccio and Thierry Billon from CEA-LETI (Grenoble, France) for providing very high quality single-domain 3C-SiC(100) samples that were essential in the success of the HREELS and SR-PES experiments. All the calculations were carried out using the in-house facilities of Materials Design, Inc. (USA) and Materials Design, SARL (France)

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CAPACITANCE OF MOS STRUCTURE BASED ON INHOMOGENEOUSLY DOPED SEMICONDUCTOR NANOWIRE

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1. Introduction

Semiconductor nanowires are promising building blocks for near future nanoelectronics since they provide a new route to continuing miniaturization as well as a wealth of opportunities in nanoscale science and technology [1-4]. They are expected to have applications in field effect transistors, sensors, solar cells and thermoelectric systems [5-9].

The vapor–liquid–solid (VLS) [10] growth process is one of the most widely used nanowire growth methods, because it offers excellent control of nanowire size [11] and composition [12]. In VLS growth, a vapor-phase precursor catalytically decomposes at a metal nanoparticle surface, forming a supersaturated eutectic liquid. The solid crystalline nanowire grows by precipitation from the liquid catalyst particle. The incorporation of intentional impurities into nanowires, or doping, is usually accomplished by introducing dopant precursor gases during synthesis [1]. During VLS growth, dopants can be incorporated into the core through the catalyst and onto the surface by uncatalysed decomposition. Given the higher surface doping, one should also consider whether dopants diffuse from the nanowire surface into the core during growth. Therefore the distribution of dopants is usually radially inhomogeneous with a heavily doped shell surrounding a core of much lower dopant concentration with a change of almost 2 orders of magnitude and the profile of dopant distribution can be different: from linear to exponential [13-15]. In this work we consider the case of power-law distribution of dopants. Understanding the surface properties and effects of dopant distribution is very important for the fabrication of high-performance nanowire devices.

2. Depletion length in inhomogeneously doped semiconductor nanowire

Formation of depletion regions at different interfaces in semiconductor homo and heterostructures plays an essential role in the physics of most electron devices.Here we consider the carrier depletion, which occurs at the surface of a semiconductor nanowire of radius R greater than de Broglie wave length, so that we can neglect all quantum size effects. Due to the carrier capture by surface states or due to the work function difference and carrier exchange between a semiconductor nanowire and a contacting material (metal or semiconductor), the surface depletion layer and the near surface potential barrier can be formed (Fig. 1). Without concerning here with the microscopic basis for the formation of such a barrier, we take the surface potential $\varphi_S < 0$ as a given value and use it as a boundary condition to the Poisson equation.

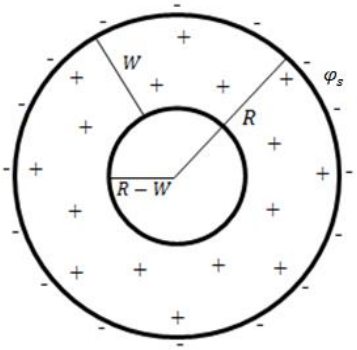

Fig. 1. Depletion region (R − W, R) in a semiconductor nanowire of radius R and surface potential φ_s.

Within the frames of the approximation of a complete and "abrupt" depletion layer of width W, the Poisson equation for the electron electrostatic potential $\varphi(r)$ in the space charge region $R - W \le r \le R$ is written as follows in the standard cylindrical coordinates:

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d\varphi}{dr}\right) = -\frac{eN_D(r)}{\varepsilon\varepsilon_0}, \qquad (1)$$

where e is the elementary charge, ε_0 is the electric constant, ε is the dielectric constant of nanowire, $N_D(r)$ is the doping density. We consider an n-type semiconductor and, for simplicity, the donors are assumed to be completely ionized at room temperature. As it has been noted in the previous section we consider the case of power-law inhomogeneous distribution of dopants, i.e. for doping density we can write

$$N_D(r) = N_D(0)(1 + \gamma(\frac{r}{R})^k), \tag{2}$$

where $N_D(0)$ is the doping density in the center of nanowire, k is the power of doping density function, γ is the parameter of inhomogeneity of doping. It is easy to show that

$$\gamma = \frac{N_D(R)}{N_D(0)} - 1, \tag{3}$$

where $N_D(R)$ is the doping density on the surface of nanowire.

By substituting (2) in (1) and requiring that at the interior edge of the depletion layer the built-in electric field and potential vanishes, i.e. $\varphi'(R-W) = 0$ and $\varphi(R-W) = 0$ (the choice of a reference point for the potential energy) andassuming that at $r = R$ the potential energy satisfies the boundary condition $\varphi(R) = \varphi_s$, we can find the relationship between the surface potential and the depletion length in semiconductor nanowire

$$\frac{\varphi_s}{\varphi_0} = \frac{x^2}{4} - \frac{1}{4} - \frac{\gamma}{(k+2)^2}(1 - x^{k+2}) - (\frac{x^2}{2} + \gamma\frac{x^{k+2}}{k+2})lnx, \tag{4}$$

where

$$\varphi_0 = \frac{eN_D(0)R^2}{\varepsilon\varepsilon_0}, \tag{5}$$

$$x = \frac{R-W}{R}. \tag{6}$$

Using (4) and (6) we can build the graph of depletion length dependence on surface potential for different laws of dopant distribution (Fig. 2). We take that $\frac{N_D(R)}{N_D(0)} = 100$ [13-15], therefore from (3) we have $\gamma = 99$.

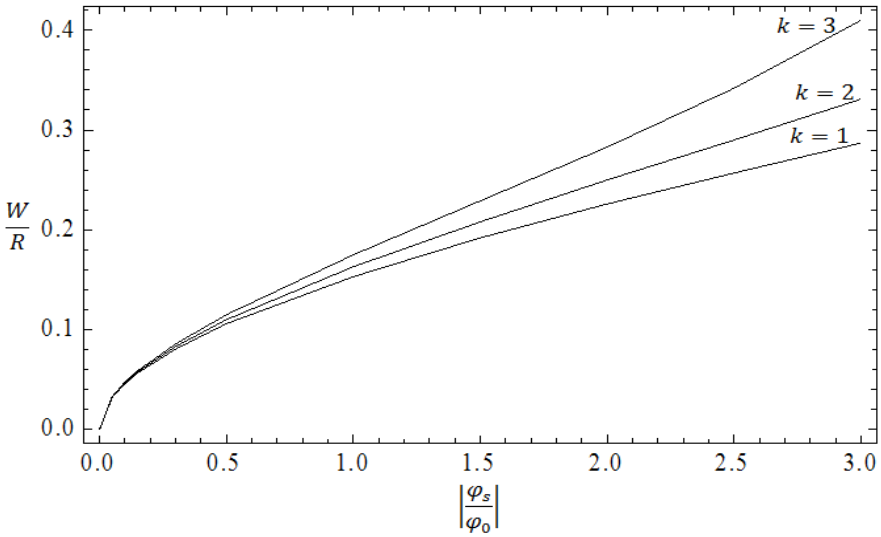

Fig. 2. Depletion length dependence on surface potential for k = 1, 2, 3.

As it is seen from Fig. 2, the law of dopant distribution in semiconductor nanowire has a great influence on the profile of dependence of depletion length on surface potential, especially at high surface band bending.

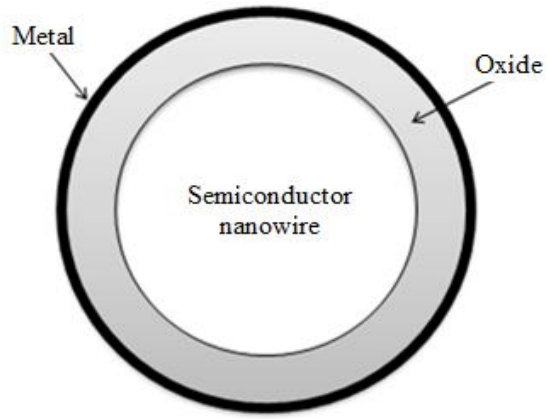

Fig. 3. Cross section of metal -oxide-semiconductor nanowire structure.

3. Capacitance-voltage characteristics of MOS structure based on inhomogeneously doped semiconductor nanowire

Next we will consider MOS structure based on inhomogeneously doped semiconductor nanowire (Fig. 3).The capacitance C of such structure in general consists of the capacitance of the cylindrical space charge C_{sc} and the capacitance of cylindrical oxide layer C_{ox} with thickness d which are connected in series, thus for C we have

$$\frac{C}{C_{ox}} = \frac{\frac{C_{sc}}{C_{ox}}}{1+\frac{C_{sc}}{C_{ox}}}. \quad (7)$$

For the capacitance of cylindrical oxide layer we have as usual

$$C_{ox} = \frac{2\pi L \varepsilon_{ox}\varepsilon_0}{\ln(\frac{R+d}{R})}, \quad (8)$$

where L is the length of nanowire, ε_{ox} is the dielectric constant of the oxide.

For the capacitance of space charge layer we can write

$$C_{sc} = \left|\frac{dQ_{sc}}{d\varphi_s}\right| = \left|\frac{dQ_{sc}}{dW}\right| \left|\frac{dW}{d\varphi_s}\right|, \quad (9)$$

where Q_{sc} is the total space charge. It is easy to show that

$$Q_{sc} = \pi e N_D(0) R^2 L(1 - x^2 + \frac{2\gamma}{k+2} - 2\gamma\frac{x^{k+2}}{k+2}). \quad (10)$$

Using (4), (6) and (10) from (9) we get that

$$C_{sc} = \frac{2\pi L \varepsilon \varepsilon_0}{\ln(\frac{1}{x})}. \quad (11)$$

In general, for a given value of potential on metal gate (φ_G), the value of the surface potential of nanowire can be determined from the equation

$$\varphi_G - \varphi_s = -\frac{Q_{sc}}{C_{ox}}. \quad (12)$$

Further, calculations are carried out according to the following scheme. For a given $\varphi_G < 0$, i.e. for a given gate voltage, we can define x from (12) (considering (4) and (10)). Then using (8) and (11) we define $\frac{C_{sc}}{C_{ox}}$ - the relative capacitance of space charge region. After that, using (7), we can define $\frac{C}{C_{ox}}$ - the relative capacitance of MOS structure, and build its dependence on φ_G. As a result, we get the capacitance-voltage characteristics of nanowire MOS structure.

For definiteness we consider the particular case of $n - Si$ nanowire covered with SiO_2 oxide layer ($R = 80$ nm, $d = 20$ mm, $\gamma = 99$). The capacitance-voltage characteristics of described structure for different laws of dopant distribution in nanowire are given in Fig. 4.

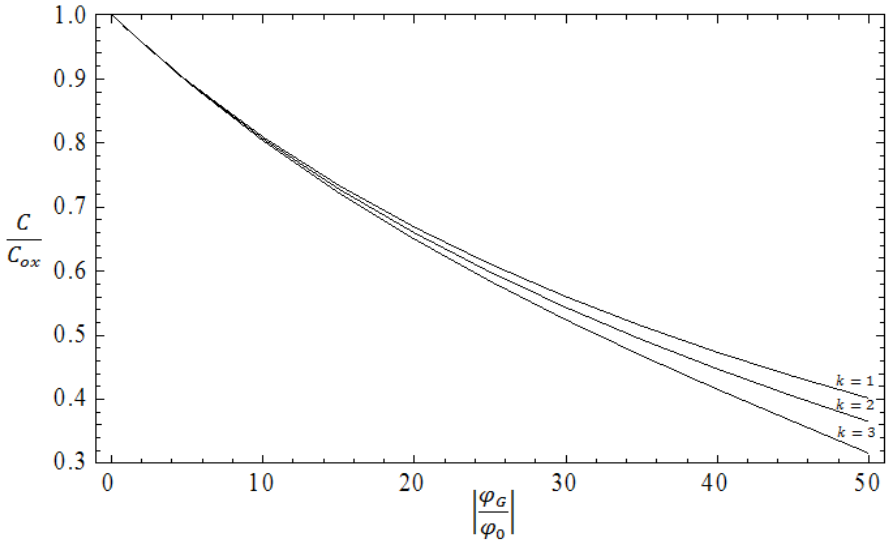

Fig. 4. The capacitance-voltage characteristics of$metal - SiO_2 - Si$structure for k = 1,2,3.

As it is seen from fig. 4, the law of dopant distribution in semiconductor nanowire has a great influence on the capacitance-voltage characteristics of MOS structure based on such nanowire. This effect should be taken into account when interpreting the characteristics of FET-based on inhomogeneously doped nanowires.

4. Conclusions

The understanding of surface band bending and dopant distribution effects is critical for the fabrication of high-quality electrical devices based on nanowires.The profile of dopant distribution in semiconductor nanowires can be different: from linear to exponential. In this work, we have theoretically investigated different types of power-law distribution of dopants. We have shown that the law of dopant distribution in semiconductor nanowirehas a great influenceon the profile of dependence of depletion length on surface potential for semiconductor nanowire and on the capacitance-voltage characteristics of MOS structures based on suchnanowires.

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EVALUATING EFFECT OF WIDTH OF NANO-CHANNEL ON BULK VISCOSITY OF L-J FLUIDS

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Abstract

Volume viscosity of Lennard-Jones fluid confined to nanochannels of different widths is calculated by employing theoretical technique based on Green–Kubo formula. Asignificant enhancement is observed in volume viscosity when width of the nanochannel is less than 10 nm.

1. Introduction

Volume viscosity also called bulk viscosity or second viscosity is considered as ameasure of resistance offered by a medium subject to forces of compression or expansion. It measures the irreversible resistance of the fluid to dilatational (volume-changing) forces. It becomes important where fluid compressibility is essential in the confinedsituations. Volume viscosity is one of the important momentum transport property, but difficult to measure experimentally. Until the present work, there exists no simulation orexperimental work for volume viscosity and longitudinal viscosity (related to shear and volume viscosity) at nano-confinement. So, it becomes desirable to seek an effective theoretical method and study the behavior of longitudinal and volume viscosities forthe fluid under confinement. Properties of fluids when they are confined to geometries of nano-dimensions are markedly different from their properties in the bulk [1–6]. As the width of the geometrybecomes smaller, interaction of fluid with the confining walls becomes increasinglyimportant. Importance of width of channel flowing at nanoscale geometry has been discussed in literature by many workers [7–12]. At micro/nano widths, fluid is inhomogeneousnear the solid boundary [13]. Transport properties of fluids have been studied andhave been found that near the walls of confining geometry these are different from that inbulk. There exists some work, which has been done on the calculation of transport properties of liquid confined in nano-channels. Sofos et al. [3] calculated the transport properties of liquid Argon flowing through nanochannel formed by Krypton walls. The effect of channel's width on shearviscosity and diffusion was studied by them [3] and it was observed that shear viscosity increases for small channel's width and it approached the bulk values as width of the channel was increased. Sun et al. [9] calculated the thermal conductivity and shear viscosity for argon-krypton (Ar–Kr) binary mixture confined in a nanochannel under Poiseuille flow by molecular dynamics (MD) simulations and found that the shearviscosity of confined mixture was higher in the confined direction. Most of the works cited above have been carried out [1–10, 13–16] on the transportproperties like shear viscosity and diffusion coefficient of confined fluids, but to our knowledge no attention has been paid to study the volume or bulk viscosity of confined fluids. Lennard-Jones (LJ) fluid is considered in the present work to study the effect of confinement on volumeviscosity. It is found that for LJ fluid volume viscosity show significant enhancement for smaller widths of the nanochannel, i.e., around 20 time the atomic diameter. Our calculations are based on themodel [19,20] which has provided reasonably good results for viscosity in a bulk fluid.

In Section 2, we present the theoretical formalism. Section 3 contains results and discussion. Conclusion is drawn in Section 4.

2. Theoretical formalism

Green–Kubo expressions for volume viscosityfor a fluid is given as

$$\eta_v = \frac{1}{Vk_BT}\int_0^\infty dtS^v(t) \tag{1}$$

,

where k_B is Boltzmann constant, T is temperature of fluid in kelvin and V is the volume ofthe system. $S_v(t)$, is volume or bulk stress auto-correlation (BSAC), and is defined as

$$S^B(t) = \frac{1}{9}\sum_a \sum_b \langle J^{aa}(t)J^{bb}(0)\rangle, \tag{2}$$

with

$$J^{ab} = \sum_{j=1}^{N} \left(\frac{p_{ja}p_{jb}}{m} + r_{ja}F_{jb}\right) - \delta_{ab}V\left(P + \frac{dP}{dE}(E - \overline{E})\right), \tag{3}$$

where a and b run over Cartesian coordinates x, y and z, N is the total number of particles,E is the total energy, p_{ja}, F_{ja} and r_{ja} are the components of momentum, force and position, respectively. Performing microscopic/exact evaluation of any of the correlation functions, S(t) andhence of viscosity is a complicated task [17-19]. However, phenomenological forms andsemi-microscopic models are available in literature [20–22], which provide acceptable predictions of viscosity of simple liquid. In this article, we have used such a model proposed by Sharma et al. [20] and subsequently used by Rohan et al. [8]. For the simplified atomic motion in liquid, we consider the correlation function to have the following phenomenological form,

$$S(t) = S_0 \sec h(t/\tau_1)\cosh(t/\tau_2), \tag{4}$$

where τ_1 and τ_2 are two parameters, with $\tau_2 \leq \tau_1$. τ_1 represents the decay of correlationfunction in an exponential manner (like low-density fluid) having structural origin whereas,τ_2 takes into account dynamical phenomena dominant at high density. By comparing shorttime expansion of Equation (4) with the exact short time expansion of S(t) given as

$$S(t) = S_0 - S_2\frac{t^2}{2!} + S_4\frac{t^4}{4!}..., \tag{5}$$

we obtain

$$\tau_1^{-1} = \frac{1}{2}\left[\frac{S_4}{S_2} - \frac{S_2}{S_0}\right]^{1/2} \text{ (6-a) and } \tau_2^{-1} = \frac{1}{2}\left[\frac{S_4}{S_2} - 5\frac{S_2}{S_0}\right]^{1/2} \tag{6-b}$$

S_0, S_2 and S_4 are the zero, second and fourth sum rules of the correlation function, respectively. Expressions of these sum rules are already known in literature [23,24] for one- and two-component fluids. To include the direct effect of confinement on atomic motion, we modify dynamical relaxation time so that it becomes a function of distance from the walls. If the effect of compression on frequency τ_2^{-1} is scaled in the same manner as it affects the frequency of oscillating particle [25-27], then

$$\tau_2^{-1}(z) = \frac{\pi\tau_2^{-1}(z=0)}{2\sin^{-1}(1-c(z))}, \tag{7}$$

where τ_2^{-1} (z = 0) is the bulk value given by Equation (6-b). Local frequency $(1/\tau_2)$ increases for a definite positive value of c(z) and for c(z) equal to zero, local frequency remains unchanged. Therefore, c(z) is taken to be $c(z) = \exp\left[-(l-z)\right]$, where 2l is the width of channel. Following the work of Rohan et al. [8] for calculation of shear viscosity of fluid confined to nanochannel, we write

$$(\tau^c{}_2)^{-1} = \frac{1}{l}\int_0^l \tau^{-1}{}_2(z)dz \ . \tag{8}$$

Here, $(\tau^c{}_2)^{-1}$ represents the relaxation time when the fluid is confined. Expression for viscosity can be obtained from Equations (1a) and (4) and is given by:

$$\eta_v = \frac{\pi}{2}\frac{nS_0}{KT}\tau_1 \sec\left(\frac{\pi\tau_1}{2\tau^c{}_2}\right). \tag{9}$$

Here, n is the number density for one-component fluid. Equation (9) coupled with Eqns. (7) and (8) will be used to calculate three viscosities by making use of corresponding sum rules.

3. Results and discussion

We consider fluid confined in z direction by two smooth walls forming a rectangular nanochannel. Fluids, which are considered here, is LJ fluid.

Effect of confinement on volume viscosity of one-component LJ fluid at two reduced densities and temperatures is studied. For calculating volume viscosity, we require values of τ_1 and τ_2, i.e., when the fluid is not under any confinement. These τ_1 and τ_2 are related to zero, second and fourth sum rules of respective stress auto- correlation functions, results for which are already available in Ref. [23] for different temperatures and densities. The calculated values of τ_1 and τ_2 are presented in the Table 1.

Table 1. Values of sum rules and relaxation time for L-J fluid for bulk stress auto-correlation functions.

T^*	n^*	S_0()	$S_2*10^{-3}(\varepsilon^3/m\sigma 2)$	$S_4*10^{-6}(\varepsilon^4/m2\sigma 4)$	$\tau_1(m\ \sigma 2/\ \varepsilon)^{1/2}$	$\tau_2(m\ \sigma 2/\ \varepsilon)^{1/2}$
073	0844	34.41	7917	102	0.06147	0.1703
1.83	0.500	47.81	37250	1607	0.03363	0.09774
3.46	0.500	119.4	147957	10720	0.02580	0.06173

Values of relaxation time, $\tau^c{}_2$ for confined fluid can be obtained from Equations (7) and (8). The values of τ_1 and $\tau^c{}_2$ thus obtained are used in Equation (9) to study the volume viscosity. Results obtained are shown in table 2 at two thermodynamic states represented by reduced temperatures and densities, i.e. for T* = 0.73 and n* = 0.844, T* = 1.83 and n* = 0.500 as a function of the width of the channel.

Table 2. Values of viscosity for different width of nano-channel (l). Viscosity is in units of 10−5 Pa s and l (in atomic diameter)

T^*=0.73		T^*=1.83	
l	η_v	l	η_v
5	11.95	5	2.86
10	8.23	10	1.47
15	5.84	15	1.25
20	5.34	20	1.1
30	5.1	30	1.08
40	5.08	40	1.05

Reduced temperature is defined as k_BT/e and reduced density $n\sigma^3$, where ε and σ are the parameters of LJ potential. It can be seen from table 2 that as we reduce width of nanochannel, the volume viscosity start increasing. For width of nanochannel up to 40σ (12 nm), the enhancement in viscosities is not significant. However, if width of channel is reduced further, viscosities start showing enhancement. It implies that for fluid confined to less than 10 nm, properties of fluids are different from that of bulk. Tendency of freezing is more in confined liquid as it is already having high viscosity. The behavior observed inconsistent with experimental/simulation observations of Zhang et al. [26], and can be attributed to the dynamical interaction between the fluid atoms and the wall.

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AHARONOV-BOHM OSCILLATIONS IN TYPE-II InAsSbP ELLIPSOIDAL QUANTUM DOTS

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1. Introduction

Semiconductor quantum dots (QDs) confine electrons and holes in all three dimensions, which lead to a δ-like electronic density of states where the energy levels are totally quantized. This property is making them attractive for optoelectronic devices not only for improved laser diodes, but also for single photon sources, quantum computing systems and new generation QD-photodetectors [1]. For lasers less temperature sensitive threshold current and emission wavelength, as well as longer wavelengths to mid-infrared region can be achieved. This also leads to an increase in infrared photodetectors response and operating temperature as well as PV solar cells efficiency. For fundamental physics and technology, some phenomena such as the interaction between coupled dots, QD/nanopits cooperative structures, and the resolution of the quantum states in current-voltage and optoelectronic characteristics have been also observed [2-6]. Among quantum size objects' fabrication techniques, the self-organized Stranski–Krastanow (S–K) method is an important one by which dislocation-free nanostructures can be produced [7]. Depending on the growth conditions, the elastic strain can be relaxed by the formation of QDs, quantum rings or even unique island-pit pairs [1,3-6]. The energies of the conduction and valence band edges of InAs, InSb, InP and their ternary alloys exhibit highly interesting electronic properties of type-II nanostructures based on them. In particular, the band offsets of InSb in InAs suggest that electrons might be located in InAs (matrix), whereas the valence band maximum is inside InSb and thus makes this material a preferred option by the hole states [1,3-6]. Along with quantum rings, type-II QDs are particularly suitable for observing the Aharonov–Bohm effect (ABE) [8], since the constituent particles of the exciton, the electron and hole, are strongly polarized in radial direction due to the spatial separation of the carriers in such systems. In our InAsSbP type-II material system, the strong localization of hole within the QD, coupled with the Coulomb attraction to the otherwise free electron in the matrix defines the ring-like nature of the system. Specifically, in a magnetic field, the electron orbits the periphery of the QD with a phase proportional to the number of flux quanta (h/e) threading the area separating the electron in the InAs matrix from the strongly localized hole in the InAsSbP QD center. Oscillations in the photoluminescence intensity of quantum rings due to the optical ABE were first predicted by Govorov et al [9]. The first type-II system to display evidence of the optical ABE was InP/GaAs QDs [10], but here, the electron is strongly confined in the QD, while the hole resides in the GaAs matrix. Optoelectronic properties of InAs/GaAs QDs were investigated by magnetospectroscopic and magnetotransmission studies accompanied by PL measurements and Fourier-transform infrared spectrometry [11]. The optical ABE has been confirmed experimentally also in a number of II–VI type-II QDs [12].

In this paper, we describe the experimental evidence of magnetoresistance oscillations in InAsSbP composition type-II QDs grown on InAs(100) substrate. Using magnetospectroscopy, we have performed investigations, which were aimed at a general understanding of the unique physical nature and properties of grown QDs, as well as to identify possible ways to control their optoelectronic and magnetic behavior.

2. Experimental procedures and characterization techniques

The InAsSbP QDs under investigation were grown on InAs(100) substrate from a quaternary composition In-As-Sb-P melt by liquid phase epitaxy (LPE) with a modified slide-boat crucible using the S–K growth mode. QDs nucleation were performed at T=550^{o}C constant temperature and contact duration of liquid phase with the substrate of 30 min. The diameter and height of liquid phase were equal to 8 mm and 150 μm, respectively. The industrial undoped n-InAs(100) (n=2×10^{16} cm^{-3} and 400 μm of thickness) was used as a substrate. According to the InAs–InSb–InP quasi-ternary phase diagram, concentrations of antimony and phosphorus in the quaternary growth solution were chosen to provide a lattice mismatch up to 3% between the InAs substrate and InAsSbP wetting layer at T=550^{o}C. The atomic force microscope (AFM «Bruker Dimension Icon» with ScanAsyst) and «Keithley-6514 System Electrometer» were used for structural characterization and magnetospectroscopy. Mesa-chips in the form of PCCs were prepared for measurements. Lateral ohmic contacts to the samples were fabricated by the traditional thermal vacuum evaporation technique in the form of Cr/Au sandwich with further thermal annealing. The geometric configuration and topology of ohmic contacts were chosen to provide uniform lateral current flow and according to PCCs requirements. The sample's active surface was chosen to be equal to 10^{-2} cm^{2}.

3. Results and discussion

AFM images of QDs grown from In-As-Sb-P quaternary liquid phase on InAs(100) substrate are collected and presented in figure 1. Structural characterization shows that QDs are sufficiently uniformly distributed in large area (~1200 μm^2) with an areal density ranging from 2 to 3×10^9 cm^{-2}. AFM line-scan characterizations (Figs. 1(*b,c*)) show that the growth process and technological conditions result in an elongation of QDs in [010] direction with an average elongation ratio of 2.5±1.

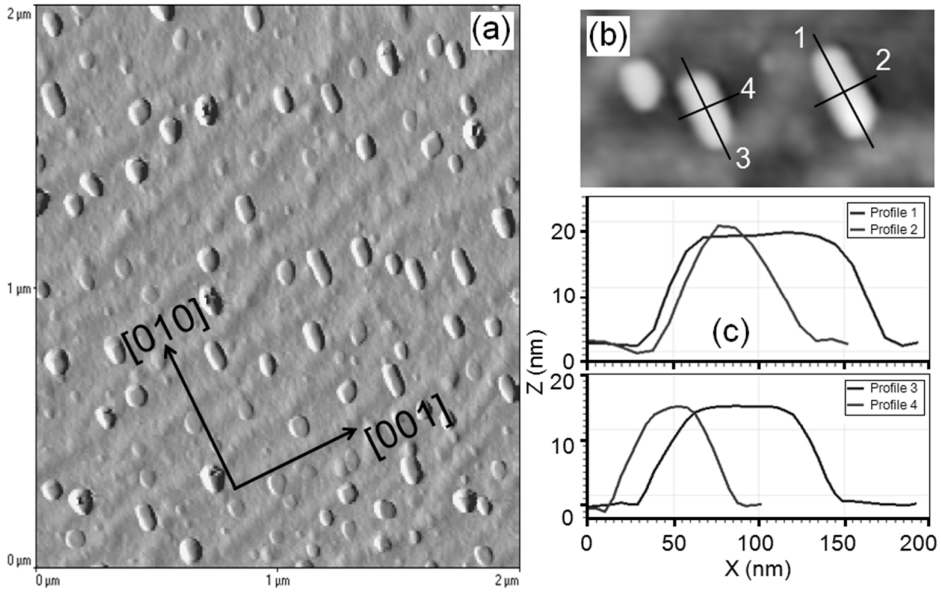

Fig. 1. AFM image (S=2×2 μm^2) of QDs grown on InAs(100) substrate from In-As-Sb-P quaternary liquid phase – (*a*); AFM image with corresponding line scans – (*b, c*).

Magnetic field dependence of the electric sheet resistance (magnetoresistance) was measured in Faraday geometry at room and the liquid nitrogen temperatures. Measurements were performed at gradually increasing of the magnetic field up to 1.6 T with further decreasing up to zero. Magnetoresistance curves for our InAsSbP type-II QDs at room and T=78 K temperatures are presented in figures 2(*a, b*), respectively. Figure 2(*c*) shows the derivative of room temperature magnetoresistance curve measured at increasing magnetic field.

From Figs. 2(*a–c*) the periodic fractures on magnetoresistance curves, oscillations of the derivative curve with the period of $\delta B \approx 0.36 \pm 0.03$ T, as well as the sheet resistance hysteresis of $\Delta R \sim 50$ mΩ ($\Delta B = 0.255$ T) and $\Delta R \sim 400$ mΩ ($\Delta B = 0.421$ T) at room and T=78 K temperatures, respectively, are glaring. Actually, type-II QDs and QRs are distinctly different from single or multiple stacked type-I QDs in that they have a not simply-connected geometry and that the charge carrier distribution is more complicated. For both cases, this geometry defines the ring-like trajectory for electrons (or holes) in magnetic field depending on band alignments. In our type-II QDs, for instance, holes are strongly localized inside the QDs, but the electron's wave function is "pushed" outside of the dot, as we have confirmed in previous calculations based on an eight-band **k·p**-simulation [3]. A schematic band structure in [001] direction and the model for an electron–hole pair in a type-II InAsSbP elongated QD in magnetic field is presented in figure 2(*d*). Evidently, the magnetic flux leads to a periodic change in the quantum mechanical properties of the encircling electrons. Therefore, upon the application of a magnetic field, the electron orbits the QD periphery producing an observable ABE. Rotation of the electron results in a periodic switching of the ground state with the angular momentum $l_e = 0$ to $l_e \neq 0$, in specific windows of magnetic field, as it is presented in Fig. 2(*c*).

However, in Fig. 2(*c*) four well-resolved oscillations with the period of $\delta B \approx 0.377$ T are evident. Since the period of oscillations should be approximately given by $\delta B = 4\Phi_0/\pi D_e^2$ [12], where $\Phi_0 = h/e$ is the quantum flux, a diameter of $D_e = 120 \pm 10$ nm is obtained. Calculated value for the electron's circling diameter is reasonable and coincides with the QDs optimal size in [010] direction (figure 1(*b,c*)). The selection rules for transitions in angular momentum are strictly valid only for the situation of perfect rotational symmetry and low temperatures (less than the temperature of thermal ionization of the exciton). Nevertheless, we assume that ABE oscillations are probable in our QDs system and that electrons perform the circular motion around the ellipsoidal QDs (Fig. 1(*b*)), since the substrate (matrix) is a high quality and undoped InAs crystal (n=2×10^{16} cm^{-3}; etch-pits density less than 10^4 cm^2), where the probability of electrons scattering on impurity or dislocation is negligibly small.

As for magnetoresistance hysteresis, detected at both room and liquid nitrogen temperatures (figures 2(*a*, *b*)), using equation $\Delta E^{hyst.} = eh\Delta B^{hyst.} / 2\pi m^*$, we have evaluated numerical values of the remnant energy, which remain accumulated in the structure after switching off the magnetic field: $\Delta E^{hyst.}$ = 1.04 meV (ΔB = 0.255 T at T=300 K) and $\Delta E^{hyst.}$ = 1.71 meV (ΔB = 0.421 T at T=78 K). Calculations were performed at $m^* = 0.028m_0$ [6]. Evaluated energies explain and affirm experimental results described in our previous work [5]. We previously showed [5] that in the similar structure, the QDs are responsible for revealed additional peaks on the photoresponse spectrum (PR) at λ=3.56 μm and λ=3.65 μm and that even at very low applied voltages ($U = \pm 1 \div 2$ mV), a sufficient increasing of the PR signal on additional peaks occurred.

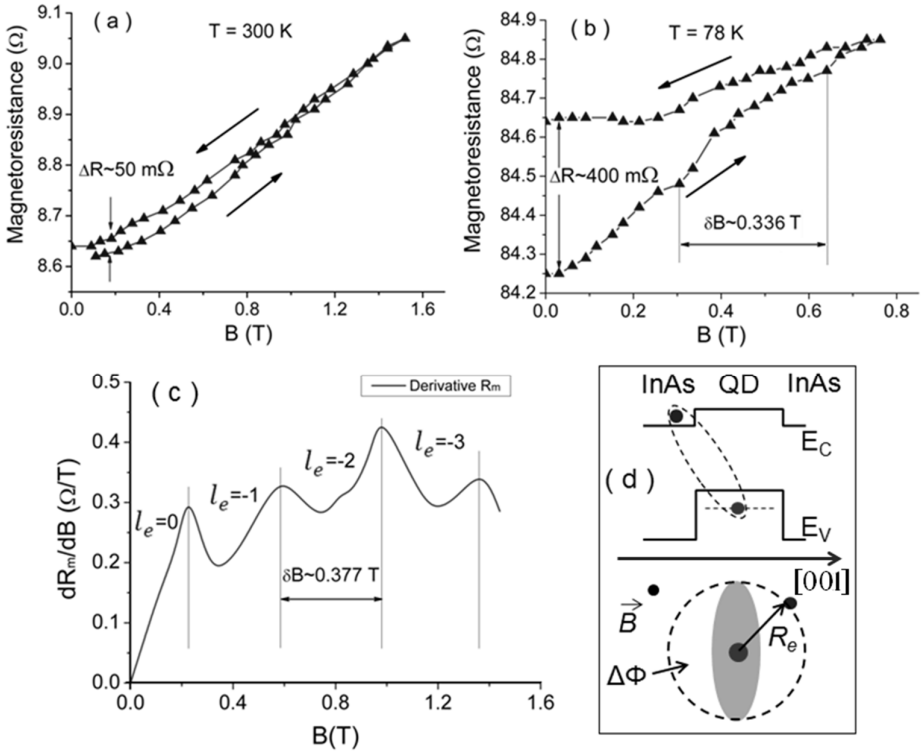

Fig. 2. Type-II QDs structure's sheet resistance versus magnetic field at Faraday (perpendicular to the substrate surface) geometry at room and liquid nitrogen temperature, respectively – (*a, b*); (*c*) – derivative of (*a*); (*d*) – schematic band structure in [001] direction and the model for an electron–hole pair in a type-II InAsSbP elongated QD.

4. Conclusions

Thus, the InAsSbP composition type-II QDs were grown on InAs(100) substrate. Aharonov-Bohm oscillations with the period of δB=0.38±0.04 T were found on the magnetoresistance curve at both room and liquid nitrogen temperatures. The magnetoresistance hysteresis equals to ~50 mΩ and ~400 mΩ was observed at room and liquid nitrogen temperature, respectively. Obtained experimental results have been explained by features typical to type-II QDs. Our study reveals a crucial influence of InAsSbP type-II QDs on magnetic and other properties of device structures based on InAs crystals, in particular, photoconductive cells and other mid- and far-infrared devices.

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GROWING, PHYSICAL PROPERTIES STUDY AND APPLICATION OF NANOSTRUCTURE CARBON MULTIFUNCTIONAL FILMS

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1. Introduction

The last decades of the 20th century was a period of unprecedented development in silicon semiconductor microelectronic technologies, devices, microprocessors, and innovative application thereof, which culminated in creation of the World Wide Web. However, by the end of the century it became clear that crystalline silicon no longer suffices for solving the problems related to the growing density of microelectronic devices and the need of heat removal, as well as manufacturing of computers with needed large memory and high speed. It was necessary to replace microelectronic technologies with nanotechnologies, and this period coincided with the advent of new carbon nanostructures and intensive research efforts were directed to the development of carbon nanotechnologies [1, 2]. In parallel, nanotechnologies based on gallium arsenide and other semiconductors were developed.

The "Heliotechnics" Research Laboratory (HRL) of the National Polytechnic University of Armenia (formerly SEUA) was established in 1986 and was involved in development and fabrication of photovoltaic devices and systems for efficient conversion of solar energy based on silicon crystals [3, 4]. Simultaneously, HRL conducted research, development and application studies of carbon nanostructure films, which are considered hi-tech. The diamond-like carbon coatings (DLC) have unique optical, mechanical and heat dissipation properties, and are stable against destructive chemical and irradiation impacts [5, 6]. The proposed film technology not only allows replacing Si in microelectronic devices and photovoltaic cells, but also substituting expensive ITO coatings in manufacturing of photonic devices. Embedding various nanostructures in carbon films through selective technological modes can create unexpected combinations of properties and numerous applications [7]. Replacement of traditional semiconductor materials with the mentioned carbon technologies and new carbon modifications will pave the way for future creation of new materials and technologies.

2. Nanostructure Carbon Film Making and Applications

Development of technologies for making DLC from gaseous phase low-temperature plasma has been described in many of our published works, such as [7, 8]. A picture of the technological equipment constructed by us for creating carbon films is presented in Fig. 1. Cylindrical vacuum chamber can be seen on the right, which has linear and radial magnetron sources used to grow the films and control their properties, as well as devices to control the plasma energy, content and film thickness during its growth. Tubes for feeding various gases and hydrocarbon vapors into the vacuum chamber are seen outside along with the flow control automated pumps, valves, measurement and regulation gauges, the overall control of which is implemented from a computer. Fully confined in the vacuum chamber, the plasma generated from inexpensive hydrocarbons and gases is used to create nanostructure films with various properties and multilayer structures that are completely intact, because they are made of only various hybridized pure carbon atoms, using clean technologies in the same vacuum chamber. Carbon generates a maximum number of allotrope modifications with both similar and contrasting physical properties (e.g. conductor graphite and graphene, or insulator diamond and carbon film). However, this technology allows changing the specific resistance of carbon film from insulating 10^{16} Ohm.cm to conductive 10^{-4} Ohm.cm by controlling the carbon film's nanostructure [7].

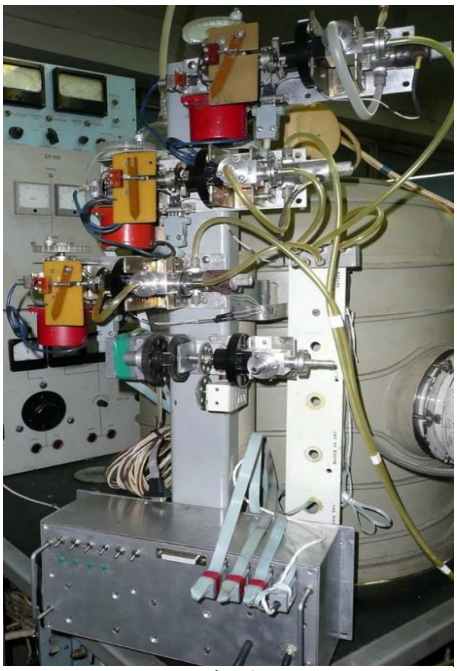

Fig. 1

Forming nanostructures in materials and especially in carbon films is a complicated technological problem, sometimes with numerous independently progressing options. Selection of the needed technological mode among the multitude of existing possibilities allows solving this problem and obtaining carbon films with necessary nanostructures and properties in a single technological setup. Through this selection we have succeeded in changing the DLC refraction indices in a wide range and depositing several layers of DLC with various refraction indices and content on surfaces of semiconductors, metals, glass and Plexiglas, and other substrates, thus increasing their optical transmittance for different applications [7, 8]. For instance, depositing DLC on the surface of semiconductors or glasses not only significantly decreases their refraction indices, but also helps protect them from aggres-

sive impacts and control their optical properties [8].

Fig. 2a and b show a wide range of spectral dependences change of DLC film refraction indices (n) contingent on technology modes of film preparation. The shown curves were built by measurements during deposition of DLC films with different properties on the surface of the same Ge crystal thin plates with p-type conductivity. Fig. 2a shows spectral curves for samples of DLC films with different dependences grown under 4 different technological modes, while in case of the same λ=830 wavelength their refraction indices change from n_1=1.4 (Curve 1) to n_4=2.8 (Curve 4). Fig. 2b shows that for the same sample it is possible to change the n from 1.4 to 2.8 in spectral range of λ=250-830 nm (Curve 1). Such large change of the refraction index in the mentioned spectral range can be used in photonics. Fig. 2a also shows replicability of spectra for refraction indices of five different samples grown under the same technological mode. As seen, in the spectral range of 250-830 nm the refraction indices differ only by 1-2 percent (Curves group 2).

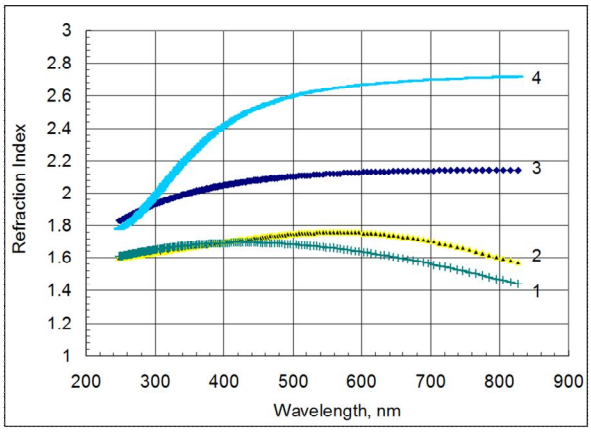

Fig. 2a

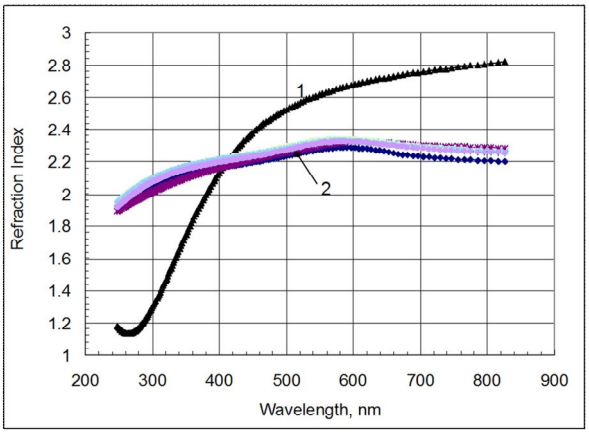

Fig. 2b

Nanostructure carbon coatings have a large demand for a variety of technical applications, such as increasing longevity of mechanical perforating, cutting, polishing and stamping tools, punch tools for making medals and other souvenirs, repair of blades and other parts that quickly wear out due to friction in internal combustion engines, generators and turbines. For example, steel surfaces of stamped medals made by applying 100 tons of pressure increase their wear resistance and useful life by several times when coated with DLC. Three- and two-layer nanostructure thin films were developed for modification of glass surfaces [6]. The entire inner surface of window glass was coated with a continuous carbon film with required nanostructures and contacts for connection to a power source. Two properties, high conductivity and high optical transmittance that are difficult to achieve simultaneously were combined in this case, which allows heating window or windshield glass by electricity in order to clean it from ice or drops of liquids, at the same time heating the interior space.

3. Conclusions

1. DLCs are active films that modify the surfaces of metals, conductors, insulators and semiconductors, protect the surface of substrates, even those of easily damaged glasses and polymers, from mechanical, chemical and irradiation impacts.
2. Embedding nanostructures in carbon films changes their specific resistances and refraction indices in a wide range.
3. The developed technology solves the problem of combining high conductivity and high optical transmittance properties that are difficult to achieve simultaneously.
4. Replacing traditional semiconductors and other materials with carbon nanostructure films may lead to emergence of many new applications and pave the way for future creation of materials with new properties and development of applied technologies.

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INVESIGATION OF THE BEHAVIOR OF POINT DEFECTS IN CdS_xSe_{1-x} SEMICONDUCTOR NANOCRYSTALS

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1. Introduction

A new branch of the semiconductor physics is related to the study of the optical and electric properties of the smallest semiconductor crystals with size of several nanometers [1,2]. Recent interest in the semiconductor nanocrystals in silicate glass has been driven by the applications in optoelectronic devices, fluorescent labels in bioengineering, and window materials in solar cells [3,4]. In comparison with bulk semiconductors, nanocrystals exhibit limitation on the motion of electrons and hence energy quantization. The positions of discrete energy levels depend on the size and shape of nanocrystals [5, 6]. The calculations of the energy spectra are normally performed with allowance for the distribution of the periodic energy potential and limitations on the motion of electrons in the presence of a periodic field. However the electron microscopy [7,8] shows imperfect crystal lattice at the initial stage of the nucleation in nanocrystals. Thus, nanocrystals exhibit both periodic and random potentials that contribute to the formation of the band structure.

In this work, we study the effect of structural defects on the optical properties of the CdS_xSe_{1-x}semiconductor nanocrystals in silicate glass.

2. Experiment

The CdS_xSe_{1-x}nanocrystals in silicate glass were fabricated using the procedure of [9]. The samples differ from each other by mean sizes of nanocrystals and degrees of perfection of crystal lattice. Two types of samples were investigated: in the first series T of samples the formation of semiconducting nanocrystals corresponded to a thermal treatment temperature of 530^0C, and the second series A of samples of 510^0C. The temperature of the heat treatment is reached over one hour, then the samples are stored at a constanat temperature (sample T_1 is not thermally processed and the processing times of samples T_2 –T_8 at a temperature of 530^0C are t_2=5 min, t_3=15 min, t_4=35 min, t_5=65 min, t_6=125 min, t_7=245 min and t_8=425 min, sample A_1 is not thermally processed and the processing times of samples A_2 –A_{15} at a temperature of 510^0C are t_2=10 min, t_3=15 min, t_4=30 min, t_5=80 min, t_6=120 min, t_7=180 min, t_8=270 min, t_9=420 min, t_{10}=510 min, t_{11}=630 min, t_{12}=810 min, t_{13}=1050 min, t_{14}=1410 min, and t_{15}=1890 min.). The transmission spectra were studied in the wavelength interval 300-900 nm using Ocean optics USB-4000 spectrometer. In this work, through the study of the optical transmission spectra to determine the behavior of point defects in the $CdSxSe_{1-x}$ nanocrystals, which are in various stages of formation. The spectral dependence of absorption coefficientthe studied samples of the range where the absorption is weak $\alpha = f(h\nu)$ has an exponential. This dependence in non-crystalline materials, known as the Urbach`s "tail".

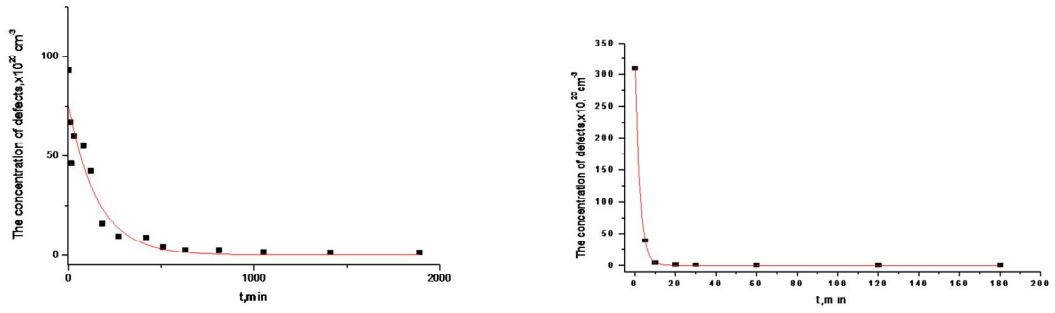

Fig. 1. Dependence of the effective concentration of defects on the heat treatment time. a) f samples T and b) for samples A.

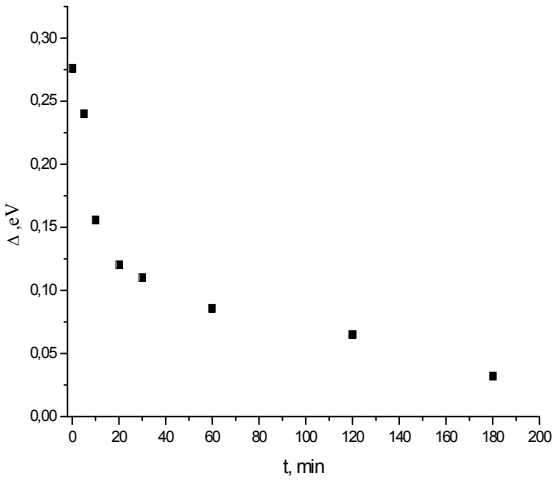

Fig.2. Dependence of the width of the exponential region of the heat treatment time for the sample series A.

The main mechanism explaining the exponential dependence is associated with the presence of disorder at the atomic level in these structures.The exponential part of the dependence $\alpha = f(h\nu)$ obeys the Urbach rule:

$$\alpha = \alpha_0 \exp \frac{-(E_g - h\nu)}{E_0}, \quad (1)$$

where E_g is the band gap, $h\nu$ is the energy of the incident photon, E_0 is the characteristic energy that characterizes the edge steepness and carries information about the standard deviation of interatomic distances. For the characteristic energy in [10] obtained a formula.

$$E_0 = 2.2 W_B (N_t a_B^3)^{2/5}, \quad (2)$$

where $W_B = e^2/2\varepsilon_{a_B}$, $a_B$is an exciton's Bohr radius, Ɛ-dielectric constant, N_t- the effective concentration of charged centers. Figure 1 a and b shows dependence of the effective concentration of defects on the heat treatment time, which was defined using formula (2), for samples T and A series, at temperature 530^0C and 510^0C.

Law changes in the concentration of defects is well described by the formula $N = N_0 e^{-\frac{t}{\tau}}$, where N_0 is the defect concentration in the samples before heat treatment, and τ is the relaxation time of defects. At a temperature of 510^0C, defects relaxation time was 158 min., and at 530^0C - 2.4 min. Such a strong dependence of the relaxation time of the heat treatment temperature recalls that the recovery process of defects has a thermal activation character. In such cases, the connection between the relaxation time and the diffusion activation energy can be written in the form

$$\tau = \tau_0 \exp(\frac{E_{diff}}{kT}), \quad (3)$$

where E_{diff} is a diffusion activation energy. Taking into account values of the relaxation times, the activation energy of diffusion of molecules dissolved in the silicate glass was determined, which is about 8 eV. The presence of defects in the nanocrystals from the energy viewpoint is equivalent to the formation of discrete levels in the band gap. Absorption at these levels is the cause of the Urbach tail. Decreasing the concentration of defects should lead to a reduction in the width of the Urbach tail. Fig. 2 shows the dependence of the width of the exponential region of the heat treatment time for the sample series A. The obtained dependences confirm the assumptions made, that is: the larger the heat treatment temperature, the faster the formation of crystal lattice in nanocrystals.

3. Conclusions

Thus, by means of optical transmission spectra investigated dependence of the concentration of point defects in nanocrystals of heat treatment time. It is shown that the recovery process of defects has thermal activation character. It estimates the activation energy of diffusion.

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RESISTANCE SWITCHING BEHAVIOR OF LITHIUM-DOPED ZnO FILM MEMORY DEVICE

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1. Introduction

Memristive switching phenomena at simple metal/oxide/ metal junctions have attracted much attention due to the potential use in high-density memory devices [1]. Memristive switching behaviors can be classified into two types: electrical polarity-dependent (bipolar, BRS) and electrical polarity independent (unipolar, URS) [2-4]. Among many materials for memristive switching, ZnO is one of the most promising due to its good transparency to visible light, adjustable electronics properties by doping of different ions, high stability and reliable memory characteristics [3]. Though excellent electrical properties such as high ON/OFF resistance ratio, good retention, and high endurance have been reported [4,5], the resistive switching (RS) mechanisms in such structures are still ambiguous. One mechanism is based on defects (ionic or electronic), in which formation/rupture of conductive filaments is related to the density and migration behavior of oxygen vacancies (V_o) or other defects [6]. Another mechanism is based on interface switching models such as the modulation of Schottky barrier, the charge trapping and discharging, and the oxidation/reduction reaction at the interface [5,7].

In the present work the RS properties of Al/ZnO:Li/LaB_6 device, in which LaB_6 and lithium-doped ZnO (ZnO:Li) films are regarded as a shallow work function metal and a *p*-type semiconductor, respectively, are studied. It is concluded that the RS behavior of the device is related to the modulation of ZnO:Li/LaB_6 barrier, which was caused by the formation of oxide interlayer between the LaB_6 electrode and the ZnO:Li film.

2. Experiment and results

(100)-oriented lanthanum hexaboride (LaB_6) films as a bottom electrode (BE) with thickness of 600 nm were deposited on glass ceramics (GC) substrates at temperature of 850 ^oC by an *e*-beam evaporation technique. Polycrystalline ZnO:Li films of 270 nm thick were deposited on LaB_6/GC substrates at 320°C with 10 at.% Li doped ZnO ceramic target by an *e*-beam evaporation. The samples were then annealed in air at 350 ^oC for 300 s. The top aluminum (Al) electrodes with a thickness of 100 nm and an area of 0.785 mm^2 were patterned on the ZnO:Li films by a thermal evaporation. Film phase composition was studied using X-ray diffraction (XRD) with CuK_α (λ=1.5418 Å) radiation (Dron-4 instrument). The elemental compositions of the samples were examined by scanning electron microscope (SEM VEGA TS-5130MM) equipped with X-ray energy dispersive microanalysis (EDS) system INCA Energy 300. Current–voltage (*I–V*) measurements were performed by saw-waveform generator (Г6-15), two multi-meters (UT 61C) and hand-made probe station. Capacitance–voltage (*C–V*) measurements of the samples were carried out at 1 kHz under bias voltages from –8 to 8 V using E7-8 digital LCR-meter.

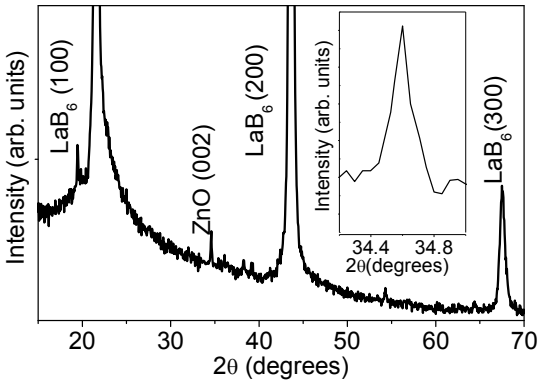

Fig. 1. The XRD ϑ–2ϑ scans data of Li-doped ZnO film deposited on LaB_6/glass ceramics substrate.

The XRD patterns of ZnO:Li/LaB_6/GC structure correspond of hexagonal ZnO film with wurtzite structure (Fig. 1). The peak at 2θ =34.6^o in the inset of Fig. 1 corresponds to (002) crystallographic orientation of hexagonal ZnO structure (JSPDS card 89-7102). The diffraction peaks at 2θ=21.354^o (100), 43.6^o (200) and 67.56^o (300) are originated from 100-

oriented LaB_6 film (JCPDS card 34-0427). No peaks of any other phase were detected. EDS analysis and following Strata-Gem software processing of the atomic concentrations of the ZnO:Li films revealed that O/Zn ratio is 1.35–1.45.

In Fig. 2 the *I–V* characteristics of the Al/ZnO:Li/LaB_6 device obtained by sweeping voltage at a rate of 0.032 V/s are presented. Each voltage sweep began from 0 V. The sweeping directions are indicated by arrows in the *I–V* curves. Fig. 2(a-d) displays *I–V* characteristics of Al/ZnO:Li/LaB_6 device for different RS states depending on cycle number.

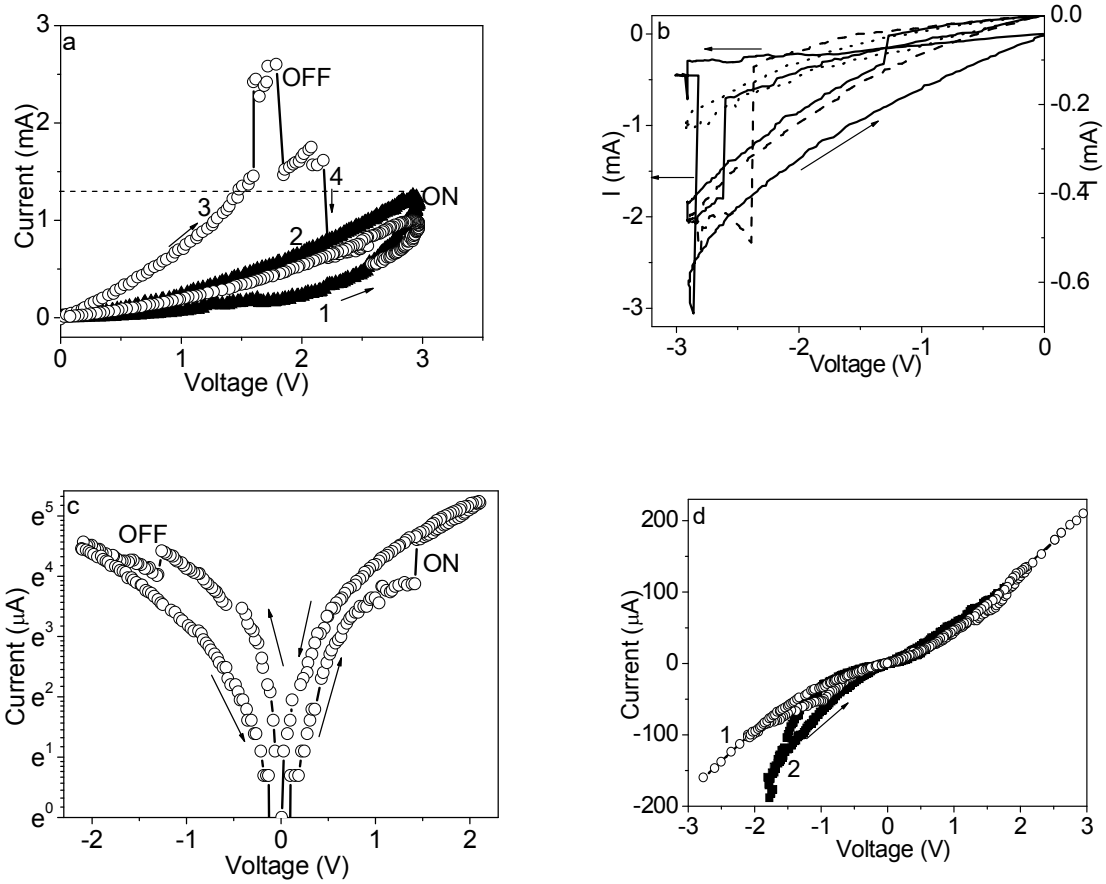

Fig. 2. The *I-V* characteristics of Al/ZnO:Li/LaB_6 device dependent on cycle number and voltage polarity. a- URS in positive sweeping voltage after 5 cycle; b- monostable threshold switching in negative sweeping voltage; c- *I –V* characteristic of BRS; d- *I –V* curves of Al/ZnO:Li/LaB_6 after cycling process (curve 3) and Al/ZnO:Li/Al (curve 1) and Ag/ZnO:Li/Al (curve 2) structures.

The bistable URS of Al/ZnO:Li/LaB_6 device for positive bias voltages is shown by the subsequent sweeping sequence along 1→2→3→4 (Fig. 2a). The film initially is in a high resistance state (HRS) until the bias voltage increased to 2.5 V, where upon the device switches to low resistive state (LRS) that can be regarded as a set (ON) state (curve 1). Next voltage application recovers the device to the LRS (curve 2).When the voltage swept to 1.85 V the current dropped abruptly (curve 3) and the Al/ZnO:Li/LaB_6 structure switches from LRS (ON) to HRS (OFF).

The resistivity ratio R_{OFF}/R_{ON} remains around 10-15 during switching cycles. Applying the negative voltage to the device in the HRS converts URS to monostable threshold switching as shown in Fig. 2(b) that recovers to the URS by applying positive voltage on the top electrode. Such reversible switching remained stable within six of switching. After 7-th cycle, the *I–V* characteristics demonstrated BRS measured in the voltage range between –2 and 2 V. As shown in Fig 2(c), the bias voltage was applied under the sweeping sequence of 1→2→3→4, and the current hysteresis indicates that a forward bias sweeping tunes the device into LRS (ON), while a reverse bias sweeping switches the device into HRS (OFF). The resistance ratio R_{OFF}/R_{ON} is ~ 2.5 and keeps more than 20 test cycles. The current decreases with the further increasing of cycle numbers, and the switching from HRS to LRS becomes difficult (Fig. 2d). Perhaps, a chemical reaction at the LaB_6/ZnO:Li interface creates a thin interlayer that blocks the charge transport or changes the effective work function at the junctions. Due to the fact that the only superstructure with La–O bonds is easy formed on the La-terminated (100)LaB_6 surface [8], one can assume that the creation of La–O bonds at ZnO:Li/LaB_6 interface induces the high density of interface states which may cause a large degree of the band bending at the ZnO:Li/LaB_6 interface, an increase of Schottky barrier height, and RS behavior change.

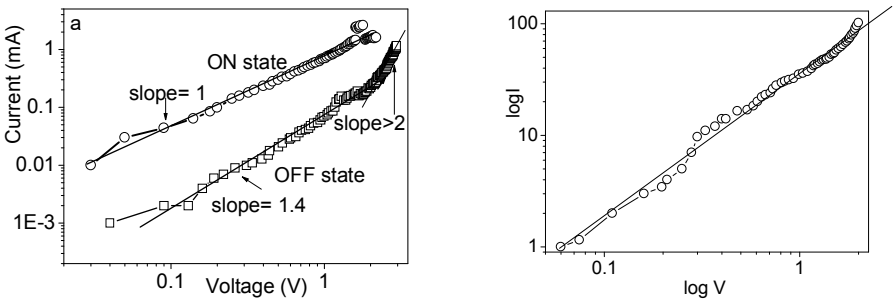

Fig. 3. The $I-V$ characteristics of Al/ZnO:Li/LaB6 device in URS (a) and BRS (b)plotted in log-log scale.

In order to know which mechanism acts in the devices, the *I–V* curves were re-plotted in a double logarithmic scale, and the linear fitting results are shown in Fig. 3. These features can be well explained by space-charge-limited current (SCLC) with a modified Child's law relation of $I \propto V^n$ (exponent n is the slope of curve) [9]. At the initial stage of the test cycles when the Al/ZnO:Li/LaB_6 device is in the URS the *I–V* characteristics of the LRS exhibit a linearly Ohmic ($I \sim V$) behavior with a slope of 1. However, *I–V* characteristic of HRS is much more complicated, which can be divided into two regions. In the low voltage range of 0–1.8 V, the *I–V* relationship shows linear dependence (ohmic) with slope ~ 1.5. When applied voltage is larger than 1.8 V, the current increases rapidly with slope 4. The characteristic of the Al/ZnO:Li/LaB_6 in BRS is linear with slopes 1.1-1.3 for LRS and HRS. The *I–V* characteristics follow Ohm's law when the density of thermally generated free carriers inside the films was larger than the injected charge carriers. In the case of strong injection, the traps are filled and the conduction becomes SCLC (Child's law).

3. Conclusions

We investigated the effect of a bottom LaB_6 electrode on the generation of resistive switching in a Al/*p*-ZnO:Li/LaB_6 structure forming a Schottky barrier. The type of RS behavior changed depending on both the polarity of applied voltage and the number of switching cycles. After a certain switching number, current –voltage characteristics exhibited RS failure, obviously low leakage current. One can assume that LaB_6-ZnO:Li reaction can introduce new dielectric layer that block charge transport or change the effective work function at the intimate junction.

Acknowledgements

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ZnO FILMS WITH *n* AND *p* CONDUCTIVITIES FOR INFORMATION RECORDING SYSTEMS

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1. Introduction

The solid-state nonvolatile rewritable memory elements are the one of the main components in information technologies. An approach based on the use of memristor effect [1-3] opens great prospects in this area. The functional area of ReRAM is about ~5 nm, which is significantly smaller than modern silicon transistor devices. Besides of storing, memristors can also implement the processing of information. In contrast to conventional elements, memristors may function both in bistable and analogue regimes of data recording and reading [4,5].

Memristor effect can occur due to the changes in the characteristics of the Schottky barrier at the metal-semiconductor interface [6]. There are other mechanisms discussed in the literature, which determine the hysteresis and nonlinearity of VAC of memristors, but all of the mare related to the stoichiometry of the oxide material and ion mobility. It should be noted that for a long time the metal oxides have been attracting attention for their unusual electrical properties that particularly become evident after the formation of the sample by electric current pulse. On this basis it can be concluded that the non-stoichiometric transparent zinc oxide films are promising for the creation of transparent memristors.

In this work we prepared and investigated 1D1R memristor heterostructures with low power consumption, consisting of a Pt/ZnO:Li/ZnO/PtSchottky diode and unipolar Pt/ZnO:Li/ZnO/ZnO:Ga memristor. We measured processes of resistance switching in bistable and analogue modes for the direct current and at a frequency of 200 Hz.

2. Experiment

There are numerous structures of 1D1R memristor memory element, in which to suppress crosstalk noises one diode 1D and one resistor 1R are used. The optimal structure for the memristors when using ZnO:Li films is unipolar schemes. The block diagram of the proposed memory element (1D1R) is shown in Fig.1. We prepared Pt/ZnO:Li/ZnO/ZnO:Ga and Pt/ZnO:Li/ZnO/Pt heterostructures by vacuum sputtering method. We designed and constructed Schottky diode (1D) based on the ZnO:Ga(40 nm)/ZnO:Li(100 nm)/ZnO(40 nm) heterostructure and memristor (1R) based on the Pt/ZnO (100 nm)/ZnO:Li (100 nm)/Al heterostructure, as well as 1D1R unipolar memristor memory element. Using these test structures, we measured electrical characteristics of 1D diodes, 1R memristors and unipolar memristor memory element 1D1R.

ZnO films were prepared by vacuum electron-beam vapor deposition on sapphire substrates coated with Pt metal layer [7]. As targets for sputtering, synthesized ceramic powder tablets of ZnO, ZnO:Li (1 %), ZnO:Li (8 %) and ZnO:Ga (2 %) have been used. All samples were fabricated using same preparation conditions: the electron energy was ~ 6 keV, the substrate temperature was maintained at 250 ± 1°C and the growth rate was 1.45 Å/ s.

Used method provides ZnO:Li films having oxygen deficiency; as a result compensated semiconductor containing both donor (oxygen vacancies) and acceptor (Li^+) centers were obtained. Annealing in air results in a change of their ratio, i. e. to the change of compensation degree.

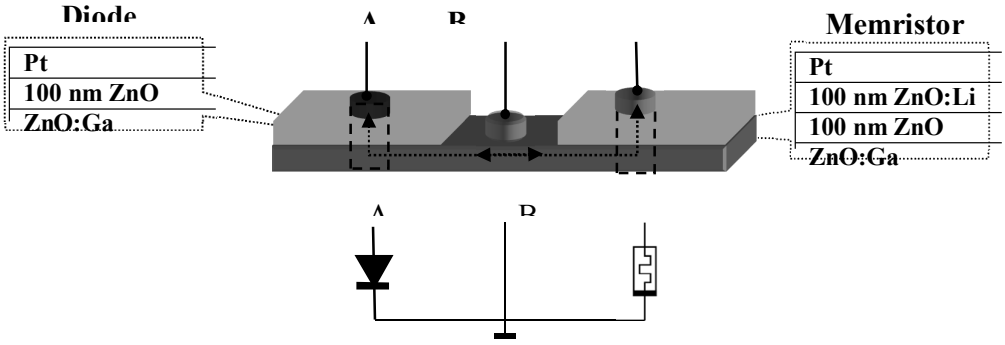

Fig. 1. Structural and equivalent schematic of the proposed structure.

The crystalline quality and orientation of the films were evaluated by X-ray diffractometry. To eliminate photochemical processes on the film surface they were covered with a protective layer of MgF_2 [8].

3. *Results and discussion*

Figure 2 shows VAC of obtained structures. Measurements were made by a sinusoidal signal with frequency $f = 200$ Hz. The results for VAC have been approximated by the formula:

$$j = j_{S0}\,[\exp(U/nU_{th}) - 1], \tag{1}$$

where j_{S0} is the saturation current density, n is the nonideality factor, which usually takes a value between 1 and 2 (for the diffusion current) and above 2 (for the recombination current), $U_{th} = k_B T/q$ is the thermal voltage, which at temperature 290°K equals to 25×10^{-3} V.

The structures have a low leakage current and almost symmetrical curve of VAC in the positive and negative regions of displacement. It is connected with a Schottky barrier Pt/ZnO transition, which is blocking electron injection. In contrast, a high leakage current and linear VAC are observed in the Pt/ZnO:Ga/Pt structures, that is connected with a nature of the ohmic contacts on the Pt/ZnO:Ga.

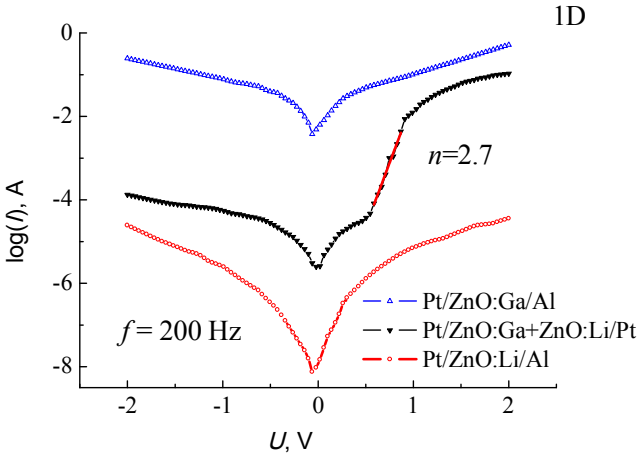

Fig. 2. VAC of the Pt/ZnO:Ga/Al, and Pt/ZnO:Li/Pt and 1D structures of the Pt/ZnO:Ga/ZnO:Li/Pt with nonlinear VA-Cand nonideality factor = 2,7

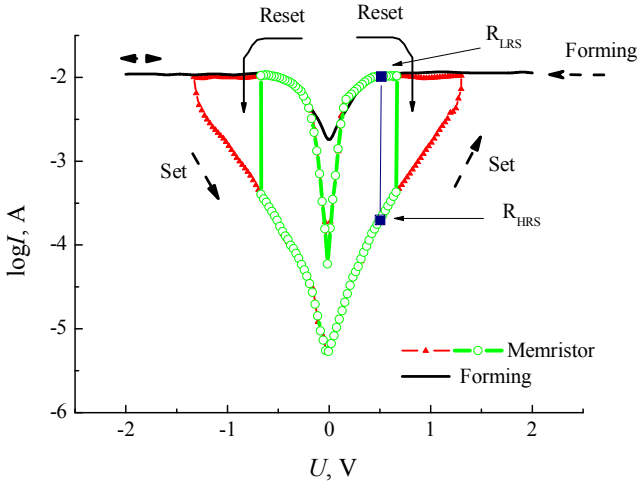

Fig. 3. VAC of unipolar memristor 1R based on Pt/ZnO/ZnO:Li/Al.

Fermi level is near to the conduction band for the ZnO:Ga films, because of this, there is a high concentration of charge carriers, which on its turn leads to a narrowing of the width of the Schottky barrier at the transition Pt/ZnO:Ga.

Consequently, electrons can easily pass through the Pt/ZnO:Ga Schottky barriers because of the tunneling mechanism. Therefore, the barrier Pt/ZnO:Ga has ohmic VAC, and transitions Pt/ZnO are Schottky barrier with nonlinear VAC. Structure of Pt/ZnO:Ga/ZnO:Li/Pt has a nonlinear asymmetrical VAC; currents at forward and reverse bias voltage are different approximately 10^3 times at a bias voltage ±2, forward voltage drop $U = 0.9$–1 V and nonidiality factor n ~ 2.7.

Figure 3 shows typical curves of VAC of unipolar resistive switch (memristor) 1R based on Pt/ZnO/ZnO:Li/Pt cells. One of the goals of this work was creation unipolar devices in which bivalence characteristics would arise only for a single po-

larity voltage. After the preparation of samples, the electric forming process was conducted at voltages which excess the operating voltage.

After the process of the formation, the electrical switching between a high resistance state R_{HRS} and low resistance state R_{LRS} was carried out using sinusoidal signal with a frequency f = 200 Hz. Switching voltage from HRS (Vset) state to LRS (Vreset) state was ±1.5 V, and in backward direction ±0.5 V. The ratio of the resistances of the cell in these states $R_{HRS}/R_{LRS} \approx 100$. In the Fig.3, arrows show the kinetics of a change of the current flowing through the contact of 1R structure.

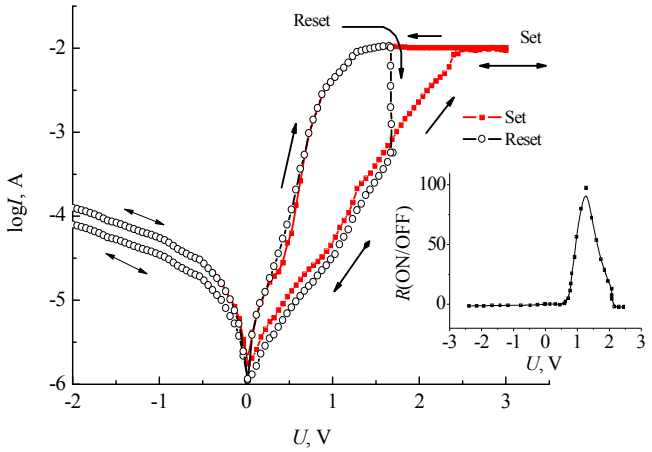

Fig. 4. VAC of the integrated unipolar resistive memristor with 1D1R structure.

Figure 4 shows typical VAC characteristics of the 1D1R integrated device, memristor 1R and diode 1D connected in series.This device also extends the initial process of the electrical formation. Switching operations in the negative bias were locked using diode with a reverse bias.

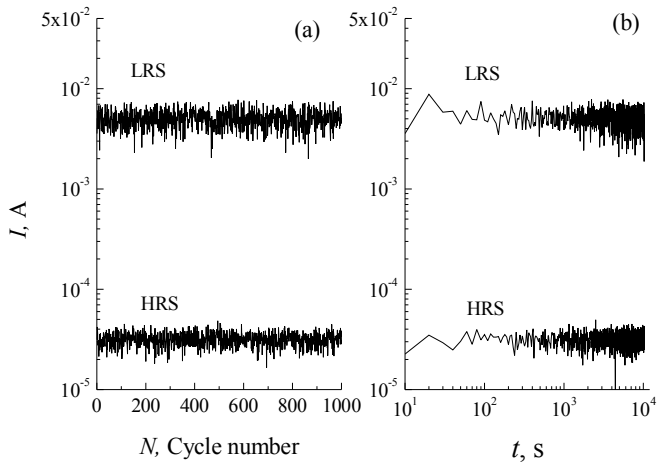

Fig. 5. Testing 1D1R device (a) in a cyclic regime of recording-reading and (b) in a regime of readout for a single time recorded data for HRS and LRS states (in case of 1 V readout voltage).

1D1R device was switching only for positive polarity of voltages, U_{set} and U_{reset} were 2.5 V and 1.7 V, respectively. From Fig. 3 and Fig. 4 it can be said that working voltages U_{HRS} and U_{LRS} of recording for 1D1R devices are higher comparing to the 1R structures because of bias voltage between diode and memristor in 1D1R device. Fig. 4 inset shows that the ratio R (ON/OFF) of 1D1R device for reading of information has a maximum value of about 80 for 1 V bias voltage. So the R_{HRS} and R_{LRS} resistances can be calculated by 1V bias voltage, which does not lead to the information loss during reading and dramatically increases number of reading cycles.

Figure 5a shows the dependence of currents for the 1D1R device in case of high HRS and low LRS resistances in a cyclic operation regime of recording-reading. As can be seen from the Fig. 5a the device allows 10^4 fold overwriting of data without a significant deterioration of parameters. Fig. 5b shows the same dependences from the reading time of single time recorded information for HRS and LRS states. As can be seen from the figure, the device without significant deterioration of electrical parameters allows to read information recorded during 10^4 seconds, assuming a single time reading 10^{-6} sec, which means that in 10^{10} - a multiple readout without derating.

4. Conclusion

We developed the new memristor memory element based on the 1D1R structure (Schottky diode 1D and memristor element 1R). 1D1R memory element switches from R_{HRS} to RLRS state and back using pulses of positive polarity, i.e. it is a unipolar memory element. The proposed device has a high stability and can withstand 10^4 cycles of switching in a writing-reading regime and 10^{10} times reading of single time recorded data without significant deterioration of parameters.

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REALIZATION OF QUANTUM FEEDBACK OF SEMICONDUCTOR THREE QUANTUM BIT NMR CELL

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1. Introduction

Quantum computers on basis of semiconductors in compare with other types have set of advantages. In particular it is easy to create enough quantity of quantum bits with their required locations and invariable hard structures [1, 2]. To this purpose it is offered to take as quantum bit the spin conditions of impurity atom ^{31}P in "spineless" semiconductor $^{28}S_i$ (Fig. 1). Here S_i is only example for demonstration of principle. For its place we can element from group A^2B^6, $S_i/S_{i_x}G_{e_{(1-x)}}$, etc. Each of these has its one disadvantage and advantages. Unary operations on quantum bits are done with the help of interaction "spin-magnetic field" (transitions between thin spectrum), but binary "spin-spin" with interaction (transitions between hyperthin spectrum). Control of this processes produced by rectangular impulses of external resonance electromagnetic field. Initialization and switching of correlation are controlled with the help of gate electric fields A and J. These systems allow doing spinor transformations in $\mathcal{H}_\kappa$ state [2, 3]. Particularly typical unary complementary operators $\hat{N}=\hat{\sigma}_x$, Adamara $\hat{H}=\frac{1}{\sqrt{2}}(\hat{\sigma}_z+\hat{\sigma}_x)$; controlled binary operators Controlled NOT $\hat{C}_N$; quantum bits state exchange $\hat{S}_w$; phase shift on φ angle $\hat{U}_\varphi$.

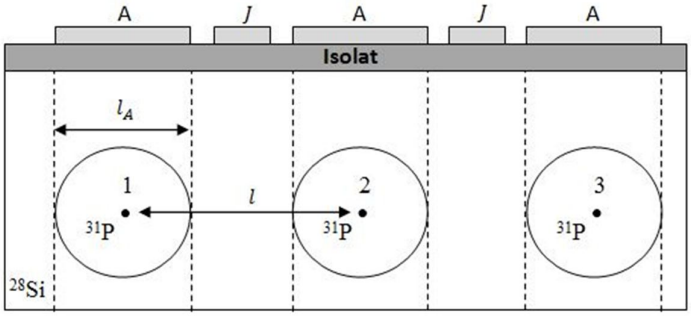

Fig. 1.

In many tasks (in iteration processes, creating strong synthetic intellect, quantum neirostorn lines, error correction and etc.) arising necessity on quantum feedback the activity condition of which on principle is not possible to know without disturbance of coherence dynamic of closed quantum system. Let $\tau=t_n- t_{n-1}$ is duration of n cycle, $\hat{U}_\tau$ unitary operator of evolution of coherent correlated quantum bit system (executable algorithm), $|\psi_n(t)\rangle$ is a vector of state in instant time t. For finding set state of quantum bit with method of many time repetition of $\hat{U}_\tau$evolution with change initial state, it is required to know in the start of every cycle difference $\big||\psi_n(\tau)\rangle - |\psi_e\rangle\big|$ without instrumentation. In [4,5] are shown that difficulty can go around if quantum algorithm of conditional feedback express with operators of cycle: if field of n cycle of recurrence state of quantum bit is not changing that is if $|\psi_n(\tau)\rangle = |\psi_{n-1}(\tau)\rangle$ than $\hat{T}$ must torn into identity operator, otherwise it must take place relation:

$$\hat{T}\begin{pmatrix}|\psi_n(0)\rangle\\|\psi_{n-1}(\tau)\rangle\end{pmatrix} \equiv \begin{pmatrix}|\psi_{n+1}(0)\rangle\\|\psi_n(\tau)\rangle\end{pmatrix}, \qquad |\psi_n(\tau)\rangle = \hat{U}_\tau|\psi_n(0)\rangle\,, \tag{1}$$

The construction and physical design of $\hat{T}$ operator is purpose of the current work.

2. Theory

Let us consider periodically substituted $^{28}S_i$ atoms in the crystal lattice in the narrow barrier of MOS system structure donor atoms ^{31}P (Fig. 1).The nuclear spins of donor atoms I_D are good quantum bits because they do not interact with the surrounding atoms $^{28}S_i$, but interact with the external magnetic field, as well as they are indirectly interacting with the spins of neighboring nuclei donors forming ultra-thin spectrum. Last limits distance between the donor atoms of the l with condition of wave functions overlap of the electrons of donor atoms (in this case, l~20 nm). In condition that $kT \ll 2\mu_B$ in magnetic field electrons of donor atoms will occupy only the lower spin states and donors themselves will remain in main orbital S-state. The present level of nanotechnology allows creating in each atom ^{31}P a conductive gate with size l_A which is divided with insulator layer with thickness of 2-4 nm. With the help of electric field of such gate, it can be implemented to individual control quantum bit. Between neighboring gates J electrodes are placed, with electric field of which's it is allowed to control the degree of overlap of the wave functions of the electrons of neighboring donor atoms. The electric potential J affects on values of spin-spin interaction exchange constant and on indirect interaction of nuclear spins. This al-

lows to "turning on/off" these interactions, with opportunity to control the conditional dynamics of neighboring quantum bits and apply quantum correlations in register. Concerned system is a good candidate to perform the basic operations of quantum calculations. In fact, the Hamiltonian of the combined system of two neighboring quantum bits on external magnetic field B is written as (in conventional notation):

$$\hat{H} = 2\mu_B B(\hat{S}_1+\hat{S}_2) - g_N\mu_N B(\hat{I}_{1z}+\hat{I}_{2z}) + J(\hat{S}_1\hat{S}_2) + A_1(\hat{I}_1\hat{S}_1) + A_2(\hat{I}_2\hat{S}_2) + \sum \hat{H}_{ico}(\omega_i t), \quad (2)$$

Here are not included dipole-dipole interactions, as it vanishes to zero after averaging over the main S-state. Then this Hamiltonian describes a four-power control system. The potentials of the electrodes A and J are included in (2) interactions constant and are responsible for managing the states of quantum bits, their correlation and formation of energy levels. The last term in the Hamiltonian (2) $\sum \hat{H}_{ico}(\omega_i t)$ describes the impact on the quantum bits external electromagnetic signals from the i-th resonant frequency ω_i and for the organization of inter-level transitions. In fact, this term describes the general information processing program in particular calculations.

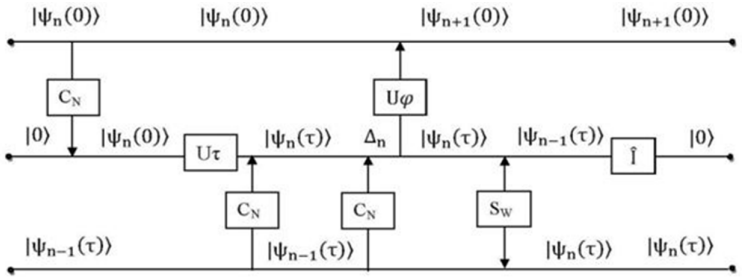

Fig. 2.

Let us have a cell consisting of quantum bits 1, 2 and 3 (Figs. 1, 2), first and third for $|\psi_n(0)\rangle$ and $|\psi_n(\tau)\rangle$, respectively. Second is an intermediate for formation of indirect coupling between quantum bits 1 and 2 as well as for perform auxiliary operations. Let us consider quantum circuit shown in Fig. 2, where the operators are functioning from left to right. Let bring in two quantum bits of "proximity" state concept (2 and 3 in Fig. 2) ratio: $\Delta_n \equiv \left||\psi_n(\tau)\rangle - |\psi_{n-1}(\tau)\rangle\right|$ (or $\Delta_n \equiv ||\psi_n(\tau)\rangle - |\psi_e\rangle|$ in the case of a comparison with peer status $|\psi_e\rangle$). Then identity $\hat{C}_N\begin{pmatrix}|a\rangle\\|b\rangle\end{pmatrix} \equiv \begin{pmatrix}|a\rangle\\\Delta_{ab}\end{pmatrix}$ determines the condition of iteration repetition cycle that is a feedback loop.

3. Conclusion

Above introduced principle of forming quantum feedback of operator $\hat{T}$ is general and is applicable also for any physical way of operation realization in papers structure $\hat{T}$. However, this operator is reversible only mathematically. Physically it is not reversible because of non unitary operations $\hat{I}$ of second quantum bit initialization when destroys its information, while trifling lost of energy is present. To decrease quantum bit state "proximity" and for improvement of iteration process convergence it can define $\Delta_n \equiv ||\psi_n(\tau)\rangle - |\psi_{n-1}(\tau)\rangle|$-ε, where ε >0 defines precision of process. In that case we must reject from resonance control in realization of that process.

In NMR computers coherent correlation of spin states saves "relatively" long, but it needs law temperatures (≤0,1°K) and strong magnetic fields (≥2 T) for significant of energy-level splitting. This difficulty partly can be overcome using "spin refrigerators" and the ensemble of variant [1,6]. Last is giving also opportunity to increase measured amplitude of final state.

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SEMICONDUCTOR CONDUCTIVITY STIMULATED IN $YBA_2CU_3O_X$ CERAMIC HIGH-TEMPERATURE SUPERCONDUCTOR AFTER A SHORT-TERM HEAT TREATMENT

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1. Introduction

The superconductor-to-semiconductor transition and its research for high-temperature superconductors (HTS) is essential and draws attention of a number of the world scientific laboratories [1-9]. First of all, such research can be used to reveal the HTSC mechanism and its practical application. It is known that this transition can be obtained by introducing various dopants [1-3, 7] or radiation defects [4-7] to high-temperature superconductors. The resistivity above the critical temperature of the superconducting transition, T_c, for the $YBa_2Cu_3O_x$ single crystal sample after synthesis and exposure to air up to 17 years increases only several times, and the T_c itself changes by a few degree (natural aging) [10,11]. It is also known that as a result of short-term heat treatment, metastable defects are formed in HTS which are constant migration - redistribute, causing certain changes of characteristic parameters of these materials depending on the exposure time t_a, after heat treatment (aging) [12]. In addition, it is shown that in YBa2Cu3O_x superconducting films after a short-term low-temperature treatment (400-700˚C) in air or in vacuum, some superconducting phases with various T_c are formed as well as a non-superconducting phase without substantial modification of oxygen stoichiometry [8]. The semiconductor conductivity was observed both in ceramic and film HTS materials [5-9, 13]. However, there is no agreement of opinion on the cause of the origin of semiconductor conductivity in HTS [9]. Previously we studied the superconducting and electrophysical properties of an yttrium compound after 30 min heat treatment at 400°C with subsequent exposure at room temperature up to t_a = 256 hours [14]. The observed increase of resistivity in normal conditions was more than two orders of magnitude and was presumably attributed to the increase of volumetric fraction of the semiconducting phase formed in the sample during aging [14].This paper presents the results on changes in the superconducting properties and stimulation of the semiconductor conductivity in the ceramic $YBa_2Cu_3O_x$ HTS after exposure to short-term heat treatment and aging for a relatively long time, t_a.

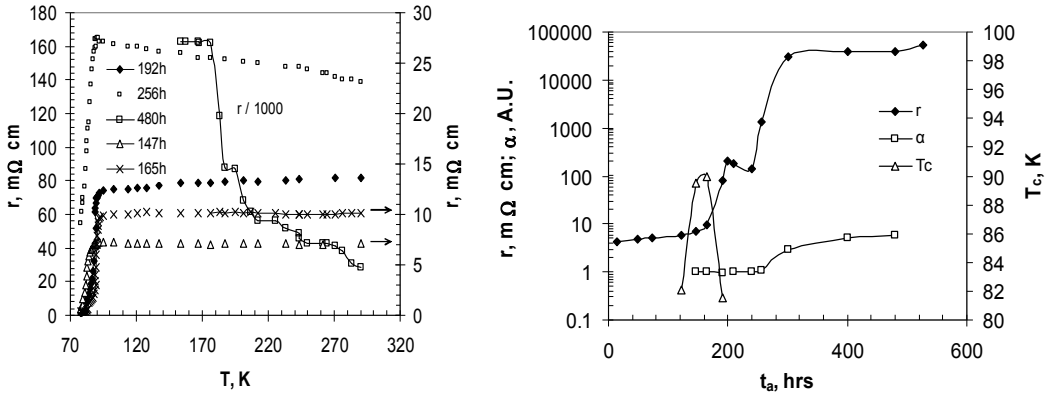
2. Experimental Methods

In our experiments, a ceramic HTS sample, $YBa_2Cu_3O_x$ (Y), was investigated synthesized in air by conventional powder technology. From the Y compound tablet (10 mm in diameter and 2 mm thick), two nearly identical rectangular samples sized 2 mm × 1 mm × 8 mm were cut. Study of the aging process was conducted by recording current-voltage characteristics using the standard four-probe technique in the presence of the Earth's magnetic field [14]. One of these Y samples was heated in a tube furnace at 400°C in air for 30 minutes, cooled in the furnace to room temperature at a rate of 3°C/min and then kept under ambient conditions up to 480 hours (20 days). The second sample was treated under the same conditions and used as a control. During the entire storage time t_a, from time to time the temperature dependence of resistivity r(T) was recorded for the samples at a transport constant current (1 mA) within the temperature range of 78 - 300K . T_c was determined from the average point of the r(T) superconducting transition temperature. It should be noted that the parameters of the control sample did not change during the whole keeping period. Also the parameter determined by α = r (176K) / r (290K) relation was controlled [4]. The larger is α, the better semiconductor or dielectric conductivity is manifested and, hence, presumably the higher is the phase volume concentration in the sample responsible for that.

3. Results and discussion

Figure 1 shows r(T) curves after the heat treatment and subsequent aging for various fixed t_a (a), as well as the r(290K), T_c and α parameters vs. t_a (1b). It is seen from Fig. 1a that r(T) dependence at $t_a < 256$ hours reveals semimetallic or metallic conductivity, while at temperatures above 90K and $t_a = 256$ hours semiconductor conductivity, and further the aging is accompanied by a significant deterioration of superconductivity with its subsequent disappearance. Later (t_a = 480 hours),

some stepped sections appear on r(T) curves testifying to non-homogeneous distribution of the forming local structural defects. With increasing t_a, there is not only an extension of superconducting transitions for the sample, but also a significant increase of **r** both in the normal state immediately after T_c and at room temperature T = 290K (Fig. 1a and b). Thus, with increasing t_a T_c increases from 82.5K, reaching its maximum (90 K) at t_a = 192 hours hr and drops sharply to 81.5 K at t_a = 200 hours (Fig. 1b). As can be seen from Fig. 1a, only after keeping of heat treated Y sample for t_a = 256 hr r(T) curve reveals a maximum at T_0 = 90K, above which semiconductor conductivity is observed, i.e. r decreases with increasing



(a) (b)

Fig. 1. A family of r(T) curves (temperature dependence of resistivity) at various aging times t_a (in hours) for the Y sample (a)**;** and T_c, r(290K) and α parameters vs. aging time t_a (b)**.** Arrows indicate the respective coordinate axes (a)**.** For the other curves, the left axis is used as a coordinate axis.

temperature. It is also seen that significant changes in T_c and r(290K) are observed at $t_a \leq 200$ hours; moreover, the sample reveals holds semi-metallic or metallic conductivity type with $\alpha \geq 1$ till t_a = 240 hours. Note that at $t_a \geq 240$ hr there is simultaneous increase of r(290K) and **α** with increasing t_a **(**Fig. 1b). The main differences in the behavior of the tested parameters are observed in the "fast" processes region, $t_a \leq$ 240 hours [15]. The fast and slow processes observed in [15] are attributed to the presence of, respectively, short and long intergranular boundaries in the sample. In our case, the rapid aging processes are explained by defect formation in a loosely bound oxygen sublattice of HTS unit cell and their further redistribution at relatively short ranges distances [14,15], whereas the slow processes also by the formation of defects in a tightly bound oxygen sublattice and their redistribution at sufficiently long distances [15]. The ceramic HTS, grain boundaries can serve as efficient accumulation areas for the formed structural defects [16]. With aging, these defects become centers of current carrier traps. Consequently, the temperature rise frees the carriers from these traps, which leads to a decrease in the sample resistance, i.e. the semiconductor-type conductivity is observed. The non-monotonic behavior of $T_c(t_a)$ curve indicates that the rapid processes in Y sample are accompanied by the phenomena of the lattice ordering and disordering. Note that for T_c increase, as in the case of aging effect stimulated after heat treatment and after the low-temperature electron irradiation, the formation and further redistribution of defects in the HTS oxygen sublattice is responsible [5,6,8,14]. Thus, in crystals with oxygen index x≈7 all O (5) positions along the **b** axis are unoccupied, whereas O (1) positions are almost completely filled and form a chain of oxygen atoms. The concentration of O (5) provisions occupied by oxygen immediately after the heat treatment is sufficiently high, and with increasing t_a oxygen atoms return to the initial O (1) positions resulting in an increase of T_c that reaches its maximum 90K at t_a = 165hr [14]. However, further increase of t_a leads to the transition of oxygen atoms from O (4) poisitions to vacant O(5) position, which is accompanied by rather rapid decrease of T_c and a sharp increase of r(290K) (Fig. 1b). Relatively rapid growth of r(290K) at this aging stage is due to the fact that the activation energy of the second process is significantly higher than that of the first process [6]. Within the interval of 240 hr $< t_a \leq$ 300 hr, r(290K) increases by more than two orders of magnitude. In this region the observed processes take place for relatively high values t_a, so the processes may be called slow. However the observed here sharp increase of r and α parameters is apparently caused by the formation of a new phase and its further evolution. This assumption is consistent with the results obtained in [4,17,18], where after the treatment in the temperature range of 380-400°C and further keeping at room temperature, the formation of different phases is observed accompanied by the loss of superconductivity up to the liquid helium temperature [12] and consequently, by a sharp increase of the HTS r. In [18] it is shown that from the ambi-

ent atmosphere water molecules penetrate into the sample, and in course of time due to the interaction with OH^- ions some phases with different oxygen content are formed which have both tetra- and orthorhombic symmetry. One possible reason for the appearance of a peak just above T_c on r(T) curve is the presence of areas with different oxygen content in the sample, which is responsible for non-uniform T_c distribution in HTS [13]. X-ray diffraction studies have shown that $(TeO)_x$ doped yttrium HTS contains two secondary phases along with the parent one [7], and with increasing **x** at a given dose of gamma radiation a decrease in T_c and increase of semiconductor properties take place in the normal conditions. This effect we observed earlier also for bismuth ceramics, when unlike yttrium ceramic, aging was accompanied only by the deterioration of superconducting properties and the stimulation of 2201 semiconductor phase with the subsequent increase in its concentration at the cost of reducing volume fraction of 2223 and 2212 high-temperature phases [19].

4. Conclusions

A 30-minute heat treatment of $YBa_2Cu_3O_x$ HTS compound at 400°C in air followed by aging at 290K up to t_a = 480 hr induces aging effect in it, i.e. the change of its characteristic parameters. At low t_a the aging first leads to a slow and then a rapid increase of r(290K) in the sample. However, the rapid processes are accompanied by non-monotonic behavior of T_c. Furthermore, in the normal state Y sample exhibits semi-metal or metal conductivity, and 256 hours later at a temperature above 90K, semiconductor type of conductivity appears. The obtained results of stimulation of the superconductor-to-semiconductor transition and detailed study of the conditions of its appearance in HTS materials are of double practical importance. On the one hand, it will promote expansion of our ideas of so far unknown HTS mechanism [5,6], and on the other hand it will find certain connections with the parameters of its normal condition. Further development of such investigations will allow developing another method of stimulating semiconductor phase in HTS compounds and determining the ways for their use for practical purposes.

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UV PHOTODETECTOR ON THE BASE OF SILICON NANOWIRES

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1. Introduction

Silicon nanowire (NW) structures may be of interest in optical films and optoelectronic device applications. One aspect that has been generally overlooked is the interaction of light of varying wavelength with nanowire assemblies on a substrate, which may have implications for future optical and optoelectronic applications. Sub-wavelength diameters and proximity, combined with submicron scale lengths, may lead to interesting optical properties such as low reflectance and high absorption. Investigations of the effect of Si-nanowire length on optical absorption showed the thickness-dependent absorptance [1].More recently, photocurrent measurements have been used to qualitatively measure thespectral absorption efficiency of individual semiconductornanowires [2].Measurementsof the broadband optical absorptioncarrying out in [3]shown higher total optical adsorption spectra of Si NW samples. Si nanowires impart a significant reduction of the reflectance compared to the solid film [3,4]. It is shown that optical absorption increasing at the decreasing of the wavelength. Unlike bulk silicon Si NWs are direct band gap semiconductors, which would make them excellent choices for optical applications [5-8]. In the other hand energy bandgap of the nanowires increase with decreasing the nanowire‘s width [5].Then it should be take part successful shift of the adsorption spectra to the short wavelength. Results of optical response of the boron-doped single silicon nanowire-based metal–semiconductor–metal photodetector presented in [9].A high responsivity, of the order of 10^4 A/W, was observed even at zero bias in a single NW photodetector with peak responsivity in the near-infrared region. The responsivity was found to increase with increasing bias and decreasing nanowire diameter. The unpackaged Si nanocrystals-based photodiode exhibits a peak photoresponse of 0.02 A/W to UV light in air [10], within an order of magnitude of the response of commercially available GaP, GaN, and SiC based photodetectors. Calculations show that the maximal values of sensitivity at the wavelength 250 nm for photodiode based on epitaxial silicon can reach 0.08–0.09 A/W [11].Noise spectroscopy and diagnostics are among the powerful and sensitive tools for studies of properties of nanosized semiconductors and different-purpose devices. Phenomenon of low frequency fluctuations of electric current in semiconductors and semiconductor devices is an object of investigations of many researchers and engineers [12-15]. Studies have shown that behavior and magnitude of low-frequency-noise in devices based on nanosize silicon differs essentially from the noise in devices based on crystalline silicon [12-15]. Note that the noise power spectral density GaN based Schottky metal–semiconductor–metal photodetectors sensitive below 350 nm remains below the background level of the system (10^{-24} A^2/Hz) up to 5 V [16]. It is shown that the response curves exhibit high visible rejection, with an UV/green contrast of about five orders of magnitude.

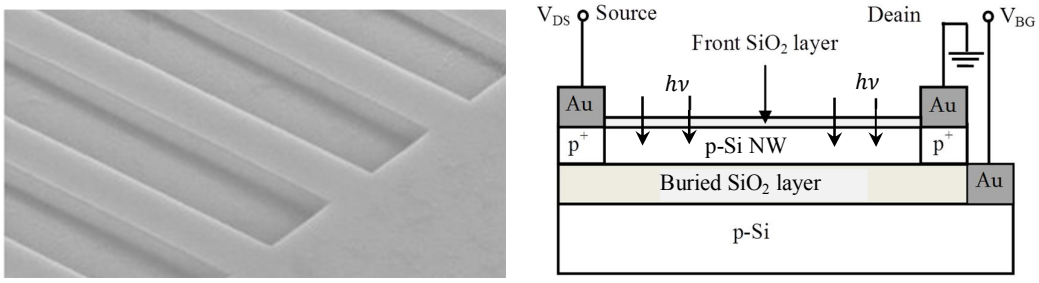
In this paper the light adsorption peculiarities and photosensitivity of the Si NW p^+-p-p^+ field-effect transistors (FET) are experimentally investigated and shows the possibility of application of this structures as a high sensitive UV photodetectors.

2. Experimental technique and results

Front oxide layer (FOX)-p/Si NW-buried oxide layer (BOX)-p/Si substrate (Fig. 1) experimental devices are made by the SOITEC- technology. Thicknesses of the layers were: $t_{FOX} = 9$ nm, $t_{BOX} = 145$ nm, $t_{NW} = 250$ nm, length of the nanowire was equal 20 μm. Device has 12 parallel NWs, which manufacture technic is presented in [17]. Spectral measurements carry out on the one NW at the 300K using monochromator YM-2. For the irradiation, we use 2 incandescent lamps remote from structure on 15 cm and irradiation densities on the NW surface in the wavelength range 0.25-0.6 μm makes up W =1.1 mW/cm^2 and 1.6 mW/cm^2, correspondingly. In Fig. 2 the source-drain dark and light current-voltage characteristics (CVC) and in Fig. 3 spectral dependencies of source-drain current are presented ($V_{BG} = V_{DS} = -5$ V). CVSs have usual form. As we can see from Fig. 3 spectral dependencies of source-drain current shift to short wavelength region as compared with bulk Si samples. Photosensitivity of source-drain current increases below wavelengths 500 nm. Note that bulk Si almost is not (or very slow) sensitive in this part of spectrum. In [2] also shown that an decrease of the nanowire diameter reveals a spectral shift of the photocurrent intensity peak towards higher photon energies, which allows tuning the absorption onset from the ultraviolet radiations to the visible light spectrum. Such behavior can be explained as follows.

- The NW thickness (250 nm) is limited absorption of the long-wave photons.
- As opposed to bulk silicon, energy gap of the nanowires increase with decreasing the nanowire‘s sizes [5].
- Internal quantum yield for Si increase and become to values 2-3 beginning quantum energy $h\nu \geq 3$ eV [18].

- As it is known [19], the color of the emitted light from the nanoscale structures is controlled by the choice of the nano-object size L, since $h\nu = E_g + E_e + E_h$, where E_g is the semiconductor bandgap energy, and the electron and hole confinement energies, E_e and E_h, respectively, become larger with decreasing L. According to the van Roosbroeck-Shockley relation, the absorption and radiation are conjugating processes [20]. The shift of the absorption spectra on the short wave range can be connected also with this fact. It is shown that these confinement (blue-shift) energies are proportional to $1/L^2$. Then with decreasing of the sizes the short wave photons can adsorbmore effectively in NWs.



a) b)

Fig. 1. Front SiO_2/-Si NW/Burried SiO_2/p-Si substrate FET structure. a) SEM image of the NWs, b) schematic picture.

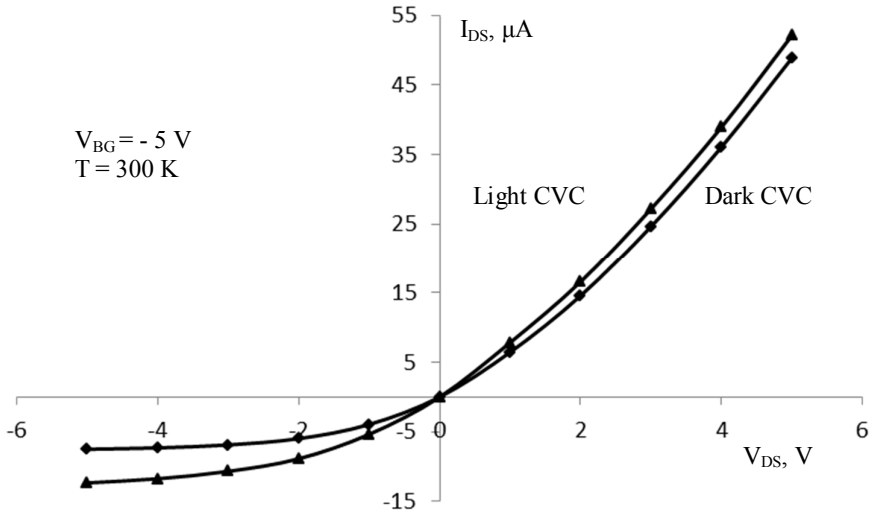


Fig. 2. Source-Drain CVC at the irradiation density W =1.1 mW/cm^2.

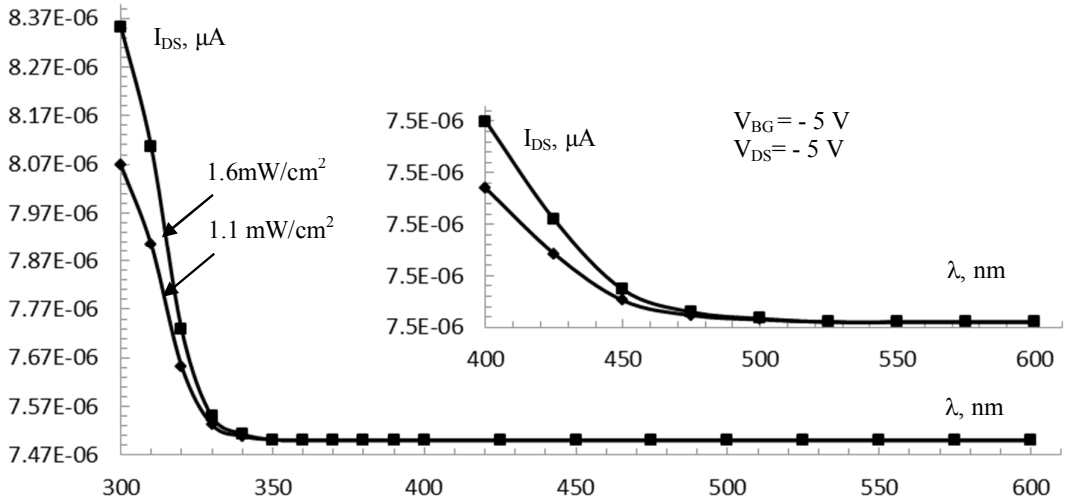


Fig. 3. Spectral dependencies I_{DS} at the several radiations of the incandescent lamp.

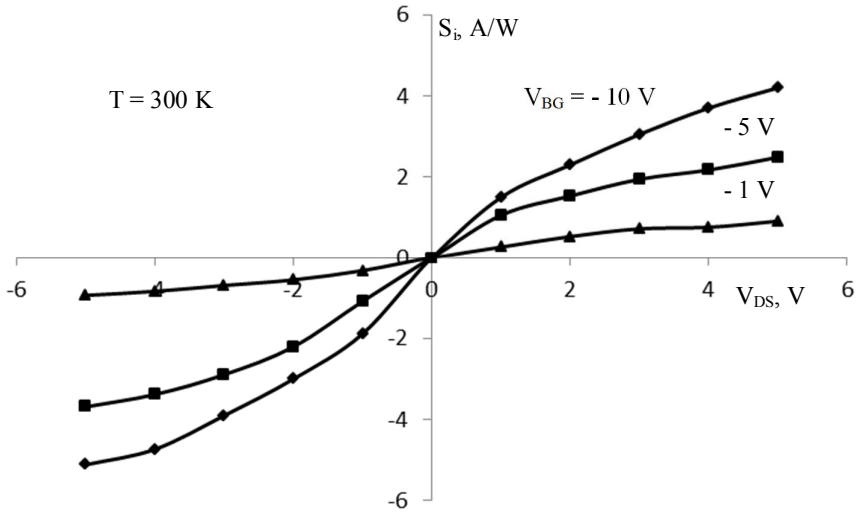


Fig. 4.Photosensitivity vs V_{DS} at the several back gate voltages.

Dependencies of the photosensitivity from source-drain voltage and spectral dependencies of the photosensitivity are shown in Figs. 4 and 5, correspondingly. Sensitivity $S_i(\lambda)$ vs source-drain voltage and its spectral dependency calculated according standard way

$$S_i = \frac{\Delta I(V_{DS})}{AW}, \qquad S_i(\lambda) = \frac{\Delta I_{DS}(\lambda)}{AW(\Delta\lambda)}.$$

Here A is the NW photosensitive surface area, $\Delta I_{DS}(\lambda)$ is the photocurrent at the wavelength λ, $\Delta\lambda = 10\text{nm}$ is the minimal feasible wavelength range.

Values of the sensitivity depending on V_{DS} reach up to 4-6 A/W at the room temperature. Sensitivity increase in the UV range of spectrum and its values about 10 time higher (see Figs. 4 and 5) than for silicon photodetectors [21-25]. Note that more low internal responsivity ~0.126 A/W at higher voltage (8 V) for a constant input optical power of 20 mW was demonstrated in grapheme FET photodetectos [26]. As opposed to our case the detection mechanisms of the device investigated in [26] werebased on photo-thermoelectric and bolometric effects.

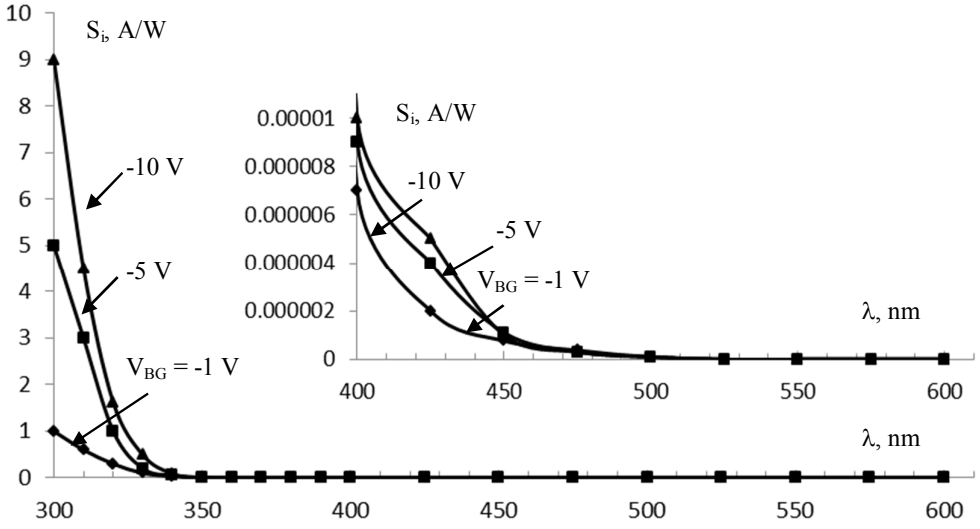


Fig. 5. Spectral dependencies of photosensitivity.

3. Conclusion

It is shown that adsorbance of silicon NW shifts to short wave region and as opposed to bulk Si photocurrent and photosensitivity reaches more high values in the UV range of spectrum at the 300K. Therefore, Si NW FETs can be successfully worked in UV range at the room temperature.

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MICROCONTROLLER MEASURER OF INFORMATIVE PARAMETER OF INDUCTIVE AND CAPACITIVE TRANSDUCERS

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1. Introduction

Inductive and capacitance sensors are widely used in a variety of information-measuring and control systems and perform the most important functions therein. Measuring devices with plunger-type inductive sensors (IS) with movable cores, in which the coil inductance increment (or unbalance of two coils' inductances) is an informative parameter, have dominated among electronic devices for linear measurements in the range of 0 ... 10 *mm* due to a number of undoubted advantages compared with mechanical devices and electric converters of other types. IS-s of eddy-current type, in which the coil resistance increment is an informative parameter, are widely used in technological process control systems in the food and pulp-and-paper industry, in brewing, pharmaceutics and biotechnologies as contactless indicators of objects' position, and for measuring the electrical conductance of fluids [1, 2]. Capacitance sensors (CS) are also widely used in automation systems for the conversion of many physical quantities and technological parameters; they are irreplaceable in measuring systems of electro-physical properties of materials and media, particularly, their moisture's [3]. The widespread use of IS-s and CS-s requires the creation of simple, precise and reliable parameters' meters of their primary transducer (PT), that are compatible with modern microcontroller devices for information processing and measurement process control. Measuring circuit (MC), which is the sensor's component along with the PT, must provide the invariance of measurement result of informative parameter of PT both to destabilizing factors affecting the PT (e.g., voltage and frequency of the feeding generator), and to its uninformative parameters.

2. Methods of research

This article describes some of the technical solutions of the problem proposed by the authors, in which structure-algorithmic methods of accuracy increase have been used. In IS-s, depending on the task, an informative parameter may be both the capacitance C_X and the equivalent parallel resistance (EPR) R_X. When measuring, for example, humidity by dielcometer method, the parameter C_X is an informative parameter, and EPS R_X is a stray parameter that shows the active energy losses that occur in the observed material placed in the inter-electrode space of PT. For this case, in the scheme (Fig. 1a) a exemplary resistor is connected in series with the PT 1. Voltage divider (VD) 2, formed by this connection, operated at a supply of the sinusoidal current of generator G (if necessary - via high-interruption-capacity element 3). The output value of MC is the phase angle φ between the voltage $\dot{U}_S$ (total voltage VD) and $\dot{U}_X$ (PT voltage). The vector diagram of MC (Fig. 1b) is built for the open position of the key *K*, where: $\dot{I}$ is the measuring current; $\dot{I}_R$ and $\dot{I}_C$ are the currents through R_X and C_X, respectively. Using vector diagram, we'll find $tg\varphi$. From the right triangle of voltages

$$tg\varphi = \frac{IR_0 \cos\delta}{U_X + IR_0 \sin\delta}. \tag{1}$$

From the right triangle of currents $\cos\delta = \frac{I_C}{I} = \frac{U_X}{x_C \cdot I} = \frac{U_X \cdot \omega C_X}{I}$, $\sin\delta = \frac{I_R}{I} = \frac{U_X}{I \cdot R_X}$, where $x_C = 1/\omega C_X$; $\omega = 2\pi f$ is the angular frequency of the generator. Substituting these values into (1), we obtain

$$tg\varphi = \frac{\omega R_1 R_X C_X}{R_1 + R_X}. \tag{2}$$

By parallel connecting a exemplary capacitor C_1 to PT (2), C_X is replaced by $\left(C_X + C_1\right)$ in (2), and for a new value φ_1 of angle φ we obtain

$$tg\varphi_1 = \frac{\omega R_1 R_X \left(C_X + C_1\right)}{R_1 + R_X}. \tag{3}$$

From Eqns. (2) and (3) a formula for the determination of C_X is obtained: $C_x = \frac{C_1}{tg\varphi_1 / tg\varphi - 1}$.

It is obvious that the measurement of an informative parameter of PT, separate from the R_X, is provided; moreover, the measurement result is not affected by the voltage and frequency of the generator. It is only necessary to measure the angles φ and φ_1, that is carried out by the same hardware.

For measuring the angle φ the electronic module 4 (Fig. 2) is used, wherein the angle φ is converted to a duration τ of single-polarity rectangular pulses. The module contains voltage followers 5 and 6, high-speed twin comparator 7 and "Exclusive OR" gate 8. Sinusoidal voltages u_S and u_X operate at the inputs of the module; at the output the sequence of single-polarity rectangular pulses is obtained, the duration τ of which is directly proportional to the angle φ. These pulses are applied to the input of the programmable microcontroller (MIC) 9, where τ is measured, φ is calculated, and using the formula (4) C_X is defined, by the value of which the current value of a physical quantity, measured by the capacitance sensor, is reflected on the digital display; MIC also controls the periodic switching of the analog key *K*.

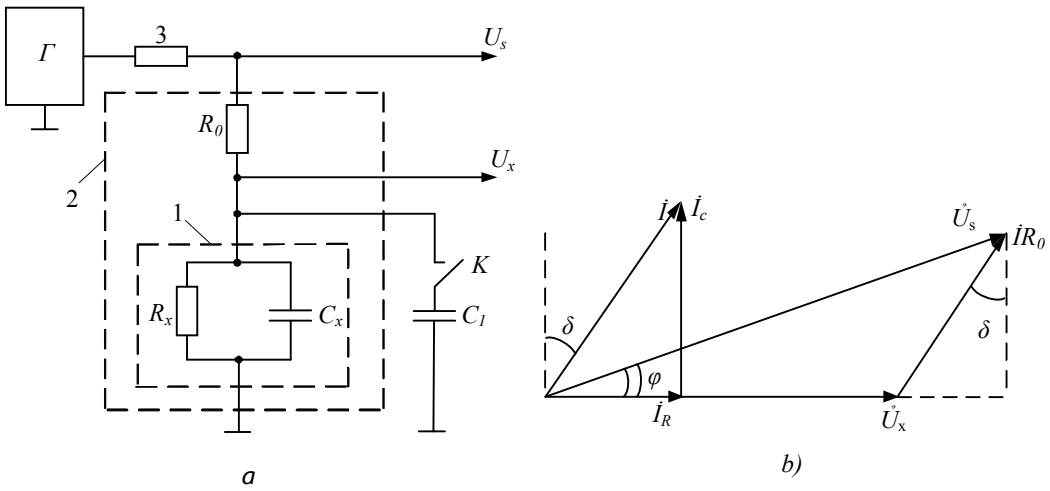

Fig. 1. Measuring circuit of CS: a) - schematic circuit;
b) – vector diagram of currents and voltages.

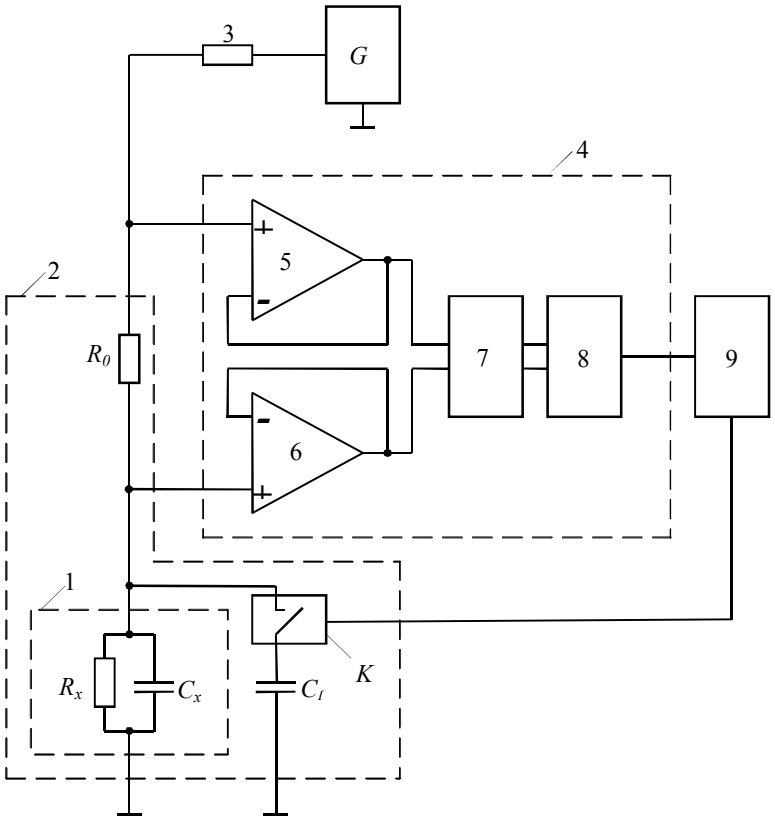

Fig. 2. Simplified block diagram of the CS capacity's meter.

The MC-s for the invariant measurement of parameters of PT IS-s act by the same operating principle. Primary transducers' coils of most modern IS-s have multilayer windings and ferrite core with high magnetic permeability. They are designed for supply with alternating current with frequency of 7-15 kHz.

In view of the surface effect, proximity effect, inter-turn capacitance, dielectric and magnetic losses, their complete equivalent circuit consists of two parallel branches and contains five elements [4]. However, at relatively low frequencies (up to several hundred kilohertz), this circuit can be replaced by a simplified equivalent circuit of the series connection of the resistor R_X and inductance L_X.

Meanwhile, depending on the task solved by IS, an informative parameter may be both L_X (in most cases), and R_X (if inductive PT is of eddy current type). The active resistance R_X of the PT depends on the frequency of current that feeds the coil due to the impact of the above effects - especially in core loss. Consequently, the parameters of the PT should be measured by alternating current frequency equal to that at which its usage is provided. Moreover, considering the non-linearity of the magnetization curve of magnetic circuit, the measuring current is also desirable to select equal to the operating current of the PT.

In developed scheme of tester of single inductive PT (Fig. 3a) exemplary resistor R_0 is connected in series with the PT. In the initial position of the switch for phase angle between the output voltages $\dot{U}_S$ and $\dot{U}_X$ the formula $ctg\varphi = \left(R_X + R_0\right)/\omega L_X$ is obtained, and in the second position of the switch - $ctg\varphi_1 = \left(R_X + R_0 + R\right)/\omega L_X$. Hence, $ctg\varphi_1 - ctg\varphi = R/\omega L_X$, from which the formula for determining L_X is obtained:

$$L_X = \frac{R_1}{\omega\left(ctg\varphi_1 - ctg\varphi\right)},$$

and from the ratio $\frac{ctg\varphi_1}{ctg\varphi} = 1 + \frac{R_1}{R_X + R_0}$ the formula for determining of R_X is obtained:

$$R_X = \frac{R_1}{ctg\varphi_2 / ctg\varphi_1 - 1} - R_0.$$

For MC of differential inductive PT (Fig. 3b) for the phase angle between the output voltages $\dot{U}_S$ and $\dot{U}_X$ in the initial and second switch positions $tg\varphi_1 = \omega L_1/\left(R_1 + R_N\right)$, $tg\varphi_2 = \omega L_2/\left(R_2 + R_N\right)$ can be written, respectively. If the unbalance of inductances (ΔL) is an informative parameter, then $L_1 = L_0 + \Delta L$, $L_2 = L_0 - \Delta L$, $R_1 = R_2 = R_0$, where R_0 and L_0 are the initial values of these parameters that are constant and known (indicated in PT's rated data). For this case:
$tg\varphi_1 - tg\varphi_2 = \omega\left(L_1 - L_2\right)/\left(R_0 + R_N\right) = 2\omega\Delta L/\left(R_0 + R_N\right)$, $tg\varphi_1 + tg\varphi_2 = \omega\left(L_1 + L_2\right)/\left(R_0 + R_N\right) = 2\omega L_0/\left(R_0 + R_N\right)$, whence the formula for determining the informative parameter of PT is obtained:

$$\Delta L = L_0 \cdot \frac{tg\varphi_1 - tg\varphi_2}{tg\varphi_1 + tg\varphi_2}.$$

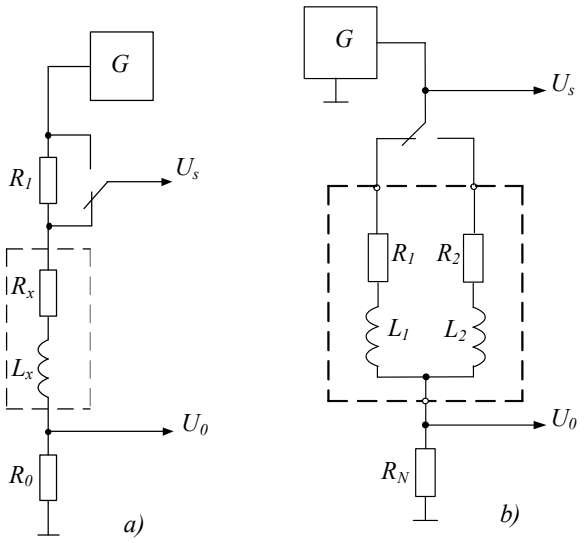

Fig. 3. MC diagram for measurement of inductive PT's parameters: unary (a); differential (b).

If the unbalance of active resistances is an informative parameter, then

$$R_1 = R_0 + \Delta R\,,\ R_2 = R_0 - \Delta R\,,\ L_1 = L_2 = L_0\,,$$

$$ctg\varphi_1 = \left(R_1 + R_N\right)/\omega L_0 = \left(R_0 + \Delta R + R_N\right)/\omega L_0\,,$$

$$ctg\varphi_2 = \left(R_2 + R_N\right)/\omega L_0 = \left(R_0 - \Delta R + R_N\right)/\omega L_0\,,$$

$$ctg\varphi_1 - ctg\varphi_2 = 2\Delta R/\omega L_0\,,$$

$$ctg\varphi_1 + ctg\varphi_2 = 2\left(R_0 + R_N\right)/\omega L\,,$$

$$\left(ctg\varphi_1 - ctg\varphi_2\right)/\left(ctg\varphi_1 + ctg\varphi_2\right) = \Delta R/\left(R_0 + R_N\right),$$

from which the formula for determining of the informative parameter of PT is obtained:

$$\Delta R = \left(R_0 + R_N\right)\cdot\frac{ctg\varphi_1 - ctg\varphi_2}{ctg\varphi_1 + ctg\varphi_2}\,.$$

3. Conclusion

The above-described MC-s provides an invariant measurement of the capacitive and inductive PT in a simple manner. Their main advantage is the exclusion of potentially-current signals, conversion and measurement of which is accompanied by the unavoidable errors caused by bias and operational amplifier's voltages, the instability of the amplification factor, the influence of the parameters of cable communication lines, etc.

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EFFECTS INDUCED IN SEMICONDUCTOR STRUCTURES BY AVALANCHING P-N JUNCTIONS

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1. Introduction

In present integrated circuits with micro- and nano-dimension elements the mutual influences of neighboring elements is a highly important problem. This influence generally is appearing as parasitic capacitive or inductive couplings. Besides that, there are some other effects induced by avalanche breakdown of local p-n junctions. These effects sometimes are much higher than the mentioned parasitic couplings. With the use of these effects new type of semiconductor devises can be developed.

The effect of conductivity modulation in Si under the impact of breakdown of a local p-n junction is investigated in papers [1-3]. It is shown that the resistivity of the channel in Field Effect Transistor (FET) is decreasing under the influence of breakdown of a locally placed p-n junction. The effect of radiation annealing in integrated circuits by breakdown of a local p-n junction is investigated in paper [3].

In this paper, the influence of avalanche breakdown of a local p-n junction on the charge carriers' mobility and the phenomenon of "photocurrent amplification" are experimentally investigated.

2. Theory

Let us consider the semiconductor structure, consisting of central p-n junction and the n – channel FET (Fig. 1). The influence of breakdown of the central p-njunction on the majority charge carriers mobility is measured with the use of magnetoresistance method. To use this method the influence of a magnetic field on the p-n junction breakdown theoretically is investigated as well. It is shown that the breakdown voltage increases under the influence of a magnetic field. Therefore, during the measurements of mobility the breakdown current is kept constant by regulation of breakdown voltage.

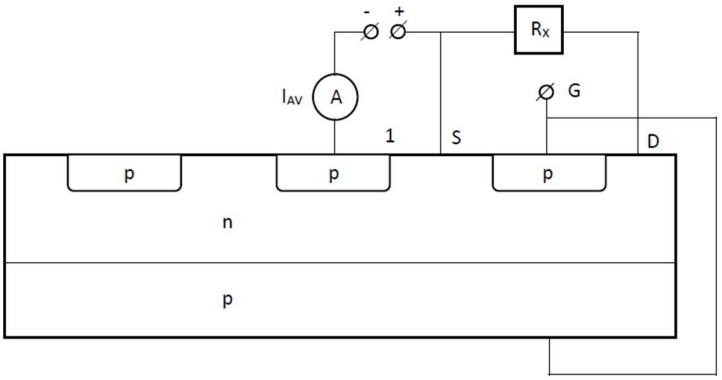

Fig. 1. Integrated circuit, consisting of central p-n junction and n – channel FET.

The measured dependence of Hall mobility of electrons in n-channel FET on the p-n junction breakdown current is shown in Fig. 2. It can be seen that the electrons' mobility is increasing with increasing the breakdown current. The mobility is increasing by about 10% when the breakdown current is 7 mA. This phenomenon can be explained by generating of acoustic phonons, which move in the same direction with electrons and effects on electrons transmission by attracting them and making the mobility higher.

The electrons' Hall mobility in the same FET when the electrons flow in reverse is measured also (Fig. 3). It can be seen that in this case the electrons' mobility is decreasing with increasing of breakdown current. The mobility is decreasing by 19% when the breakdown current is 7 mA. This can be described by opposite movement of acoustic phonons in comparison with the movement of electrons in n – channel and resisting to drift current of majority charge carriers.

Thus the mobility of electrons in the channel of FETs can be increased or decreased by the breakdown current of a local p-n junction placed nearby the FET.

The influence of breakdown of a local central p-n junction 1 (Fig. 4) on the photocurrent of the other registration p-n junction 2 in integrated circuit is investigated. The structure is illuminated by monochromatic and modulated light. The signal of photocurrent of the junction 2 is measured on the load resistant with the use of lock-in amplifier and voltmeter.

Experimentally obtained dependence of photo signal on the breakdown current of central junction 1, for one of samples, is presented in Fig. 5. It can be seen that the photocurrent increases up to 20% with increasing of breakdown current. This

"photocurrent amplification" phenomenon can be described by generating of acoustic phonons and attracting the minority charge carriers (holes) generated in the area between p-n junctions 1 and 2 towards the junction 2. After passing the maximum point, the photocurrent is decreasing and becoming even smaller than the initial value, when the breakdown current is high (4-5 mA). This phenomenon is described by removing of holes from the outer side of p-n junction 2 by acoustic phonons with high energy.

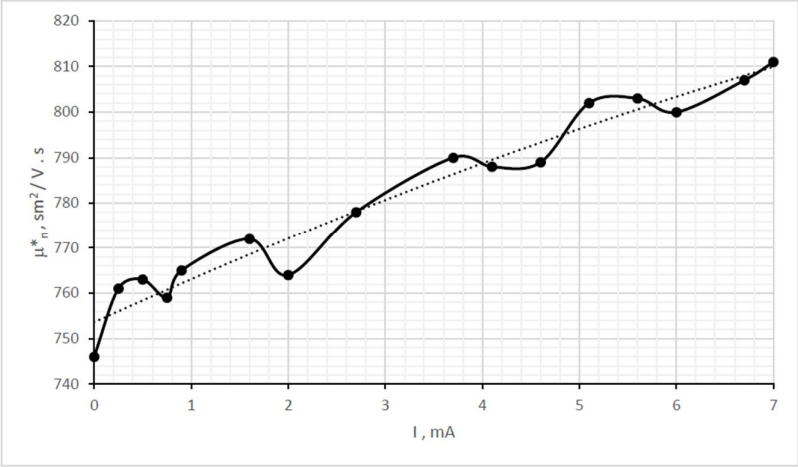

Fig. 2. Hall mobility of electrons in n-channel FET versus central p-n junction breakdown current, when electrons flow from source to drain.

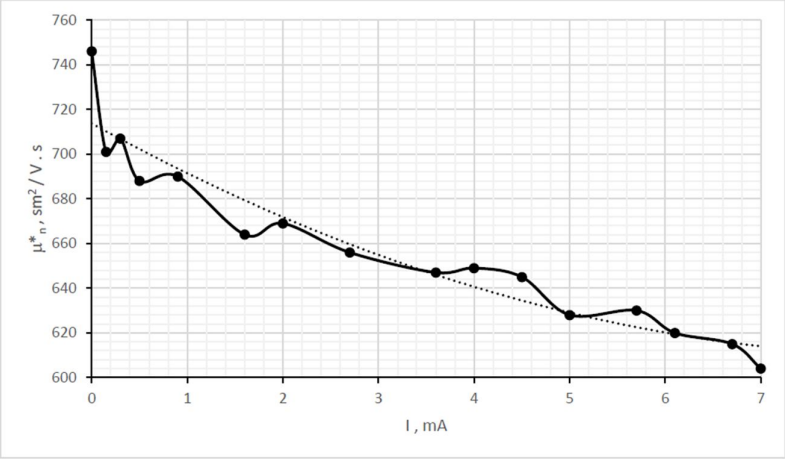

Fig. 3. Hall mobility of electrons in n-channel FET versus central p-n junction breakdown current when electrons flow from drain to source.

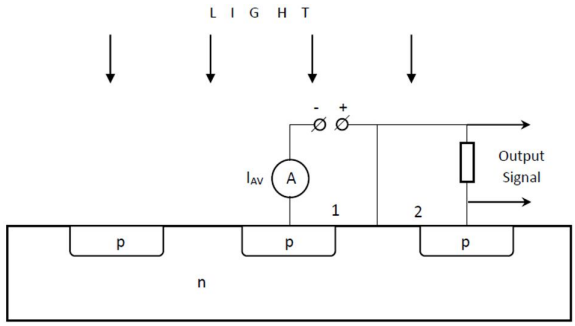

Fig. 4. Integrated circuit, consisting of central p-n junction 1 and registration p-n junction 2.

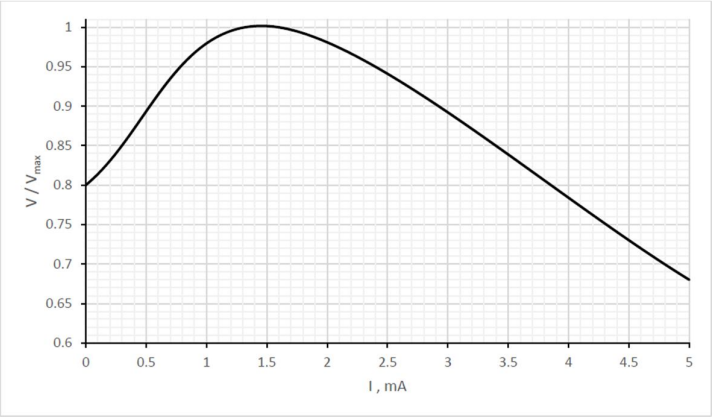

Fig. 5. Relative change of photo signal in dependence of central p-n junction breakdown current.

3. Conclusion

Under the influence of avalanche breakdown of a local p-n junction in integrated circuits the mobility of majority charge carriers in semiconductor can be increased or decreased depending on direction of movement of charge carries in comparison with local p-n junction. The photocurrent of the registration p-n junction can be increased also by breakdown of local p-n junction.

Taking into consideration also the effect of radiation annealing in integrated circuits by avalanche breakdown of a local p-n junction, it can be concluded that the p-n junction breakdown effect on neighboring elements is very important. It can be used for mobility modulation, photocurrent amplification and radiation defects annealing in different integrated circuits and semiconductor structures.

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SOLAR/WIND HYBRID POWER SYSTEMS OPTIMAL DESIGN

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1. Introduction

The development of cost-effective renewable energy systems,as the solar photovoltaic (PV) and wind systems, is important task with high environmental and social benefits. These systems consist of different components and generally it is difficult to define optimal parameters of each component to obtain the cost-effective solution. The design is more complicated in the case of hybrid solar and wind systems. To solve this problem new software program PVWind for solar-wind hybrid power systems optimal design is developed and presented in this paper. The PVWind software allows optimizing and getting the solar-wind hybrid power system having minimal price and supplying the required electric power. During design, to get the hybrid system with minimal price, the program is selecting optimal power of PV and wind components taking into consideration the available solar radiation and wind resources of a given geographical location.

The PVWind software has a user friendly interface. It has an accurate geographical location database with solar irradiations and wind speeds data. It has the databases for components as the PV modules, wind turbines, batteries, inverters and charge controllers. The user can add the new items to existing lists of components very easily. During the design, the user inputs the power and the duration of operation of AC (alternative current) and DC (direct current) loads. The user can select the desired types of components from the databases. During optimization, the program selects the optimal combination of components which is providing the minimal price for a photovoltaic-wind hybrid system.

The program optimizes the tilt angle of PV modules for desired period of year for a given geographical location. Using NASA's database [1] the monthly average solar direct radiation on horizontal surface and diffuse radiation are retrieved. To optimize the tilt angle of solar PV modules PVWind software uses the method of Liu and Jordan [2-4]. By changing the tilt angle between 0 and 90 and calculating the total solar irradiation for each tilt angle, the optimal angle is determined when the output of PV modules is maximum. The economical assessment tool of program allows evaluating the efficiency of the hybrid system by getting the total price of system, price per Watt, annual electricity to be produced, income per year and payback time. The related charts and graphs are shown in a clear approach. Thus, the "PVWind" software is an efficient and user-friendly program, which allows designing the cost effective photovoltaic-wind hybrid systems (Fig. 1).

Fig. 1. Homepage of the PVWind software.

2. Inputting parameters

The inputting parameters of PVWind software are:

Systems type - Three different systems are available for optimal design:Solar PV (only solar);Solar PV/Wind (hybrid) and Wind (only wind). At the beginning the system type is selected. Then the program will run in accordance with the selected system type. By default the system type is the Solar PV/Wind hybrid system with battery backup (Fig. 2).

Location - the geographical location is selected by inputting the country and city. According to selected location, the program selects from the data base the longitude and latitude, solar irradiation and the wind speed on the elevation of 10 meters above the ground by default and displays on the right side of the window. The user can input the other necessary eleva-

tion for the wind turbine in the range from 5 to 60 meter above the ground. The program will determine and present the wind speed for that elevation which will be used further in design process.

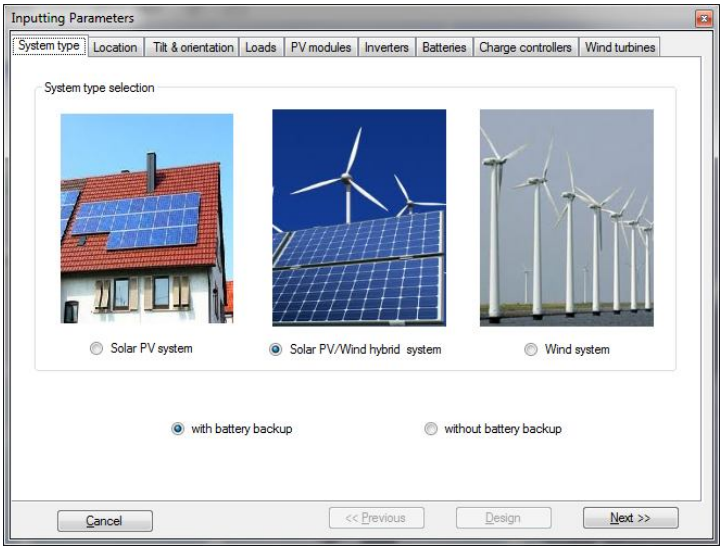

Fig. 2. System type selection inPVWind software

Tilt and orientation – the user can input the needed tilt angle and orientation of PV modules. It is possible also that the PVWind automatically calculates the optimal tilt angle.

Loads - the user inputs the parameters of AC and DC loads which will operate by electricity generated by "Solar PV", "Solar PV/wind hybrid" or "Wind" system. The input parameters for loads are the load's name, power, quantity and the working hours per day, week or month. According to these input parameters the program calculates the daily energy demand which is used further for design.

PV modules - the user selects the desired PV modules or all types of PV modules from the list. During optimization, the program selects the optimal model of PV module, which provides the required electric energy and the minimal price of the system.

Inverters - for AC loads the inverter is necessary to convert the generated DC into AC. The user selects the desired inverters or all types of inverters from the list.During optimization, the program selects the optimal model of the inverter, which provides the minimal price of the photovoltaic-wind hybrid system.

Batteries - batteries are required for the system autonomy operation. The user selects the desired batteriesor all types of batteries from the list and inputs the needed autonomy operation days. During optimization, the program selects the optimal model of battery, which provides the minimal price of the system.

Charge controllers - the charge controller adjusts the charging process of batteries. The user is selecting the desired charge controllersor all types of controllers from the list. During optimization, the program selects the optimal model of charge controller, which provides the minimal price of a system.

Wind turbines – the user selects the desired types or all types of wind turbines from the list.During optimization, the program selects the optimal model of wind turbine which provides the required electric energy and minimal price of photovoltaic-wind hybrid system.

3. Obtained results

By clicking "Design" button the software analyzes the meteorological parameters (the average solar radiation and wind velocity) of the selected location, tilt and orientation, quantity and power of each required device from the database step by step and compares the prices of each system to find the optimal system. As a result of this analysis software finds the optimal system with minimal price and presentsthe system diagram and parametersof each component (Fig. 3).

More detailed parameters of system components as well as the economic analysis can be viewed from toolbar. The PVWind program allows viewing and comparing the costs of different systems with different combination of components (Fig. 4). Each bar chart includes three colors. The sky blue color is devoted to wind turbine and its cost, the orange color is for photovoltaic module and the pink color shows the other components costs such as the battery, inverter and charge controller. The power of different systems is also presented in a graph.

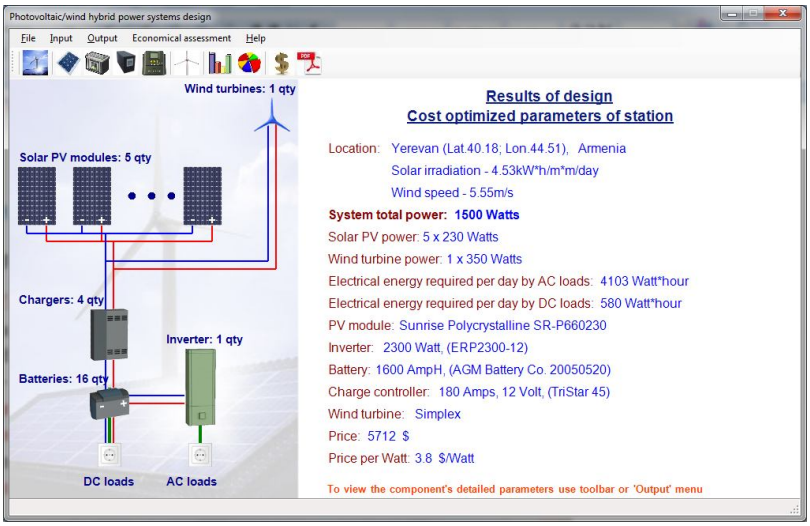

Fig.3. Obtained parameters of system and electric diagram.

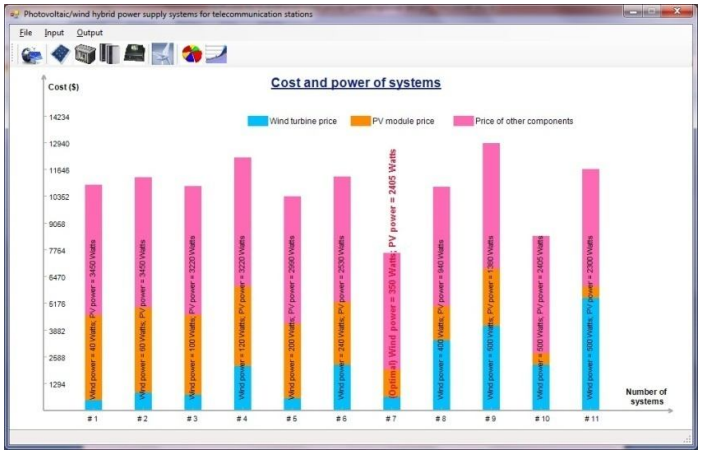

Fig. 4. Graph of costs of different systems analyzed by PVWind program.

It can be seen from Fig. 4 that the system No.7 with minimal price is chosen by software as an optimal version. The program calculates main economic parameters of the designed system as well.

4. Conclusion

The PVWind software presented in this paper is designed with consideration of accurate geographical and technical specifications. PVWind software enables users to design cost effective solar-wind hybrid power systems with minimum price. It is an efficient program that allows the user to work without any difficulties as the related charts and graphs are shown in a clear approach. The applications of this software are very wide. It can be used by designers, engineers and researchers for design of stand-alone cost-effective solar-wind hybrid power systems for homes, hotels, hospitals, schools, telecommunication systems, etc. The PVWind software can be used for educational purposes at universities as well.

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BATTERY OPERATED DOSIMETER WITH TEMPERATURE BASED ERROR COMPENSATION

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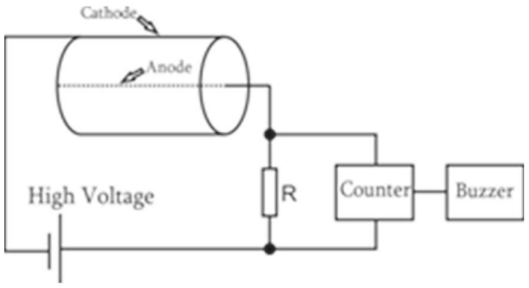
1. Introduction

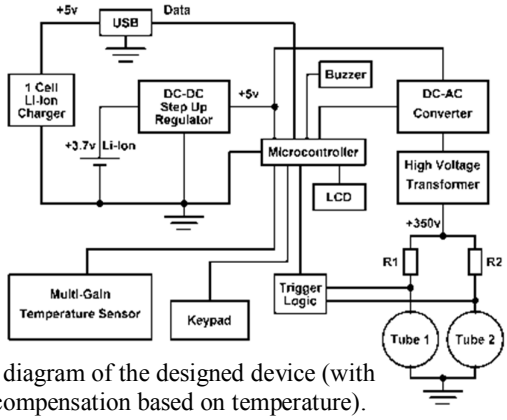
Availability of radiation exposure measurement equipment in different fields of science and even everyday life is essential. There exist different devices that provide information on environment radiation exposure, from pocket sized dosimeter pens to desktop devices. Small portable models (such as PEN2R, PEN5mSv) present live radiation reading, and are not designed to interface with other devices such as for storing and analyzing information. More advanced devices (such as GeGi) that allow connectivity features are also available, but they are not portable and are quite expensive. Of course, the above mentioned devices are designed to serve different purposes, but none of them can be used in this research project as a portable dosimeter with low power consumption that can be set and controlled from a computer. After a search for such a device that meets the project needs, it becomes clear that a custom one needs to be designed to satisfy all the parameters of the research.

2. Device structure and operation

The concept of the well-known Geiger counter [1] lies in the base of the device.The classical Geiger counter consists of a tube filled with inert gas such as helium, argon or neon, in some cases a Penning mixture, and a quench gas of 5-10% of organic vapor or halogen gas to prevent multiple pulsing. Also,a buzzer or a light emitter (in some cases both)is present as a notification method for the operator. The tube is built from glass or similar material, which has two electrodes, one of which is the thin wire going across the tube (anode), and the contacts on the sides or one side of the glass (cathode). Using the high voltage transformer, a pre-adjusted fixed voltage is applied to the tube electrodes. The voltage for most of the common devices is a couple of hundred volts. When a particle passes through the tube, the gas is being ionized and a certain current passes through anode and cathode. The current causes a voltage drop, which is used to trigger certain logic to make the buzzer beep and the light to turn on. So for every particle passing through the tube, a short beeping and a short flash of light occurs for the operator. Block diagrams of the simple Geiger counter,the one that has been designed for research purposes that includes error compensation based on temperature is shown in Fig. 1.



Block diagram of a basic Geiger counter.



Block diagram of the designed device (with error compensation based on temperature).

Fig. 1. Basic Geiger counter (left) and the updated device (right).

The new dosimeter has been developed based on the older model, but with added readout features, and more precise measurement technique. The device, again, consists of two gas tubes, instead of one, which increases the detection sensitivity. Depending on the particle angle and the direction it comes from, it can be absorbed by the body parts of the detector device or not meet the tube surface at all [2]. So, by making the detection surface larger, the possibility of detecting particles and the quantity of detected particles in a certain given time window increases. As a power source for the circuit's operation, astandard mobile phone battery is used. It runs the device continuously for more than a week, without the need to charge it.

Using a DC-DC step-up IC (MAX1674, Fig. 2), the 3.7 volts of the battery is converted into 5 volts, which is used for the most logical elements of the circuits, including the microcontroller.

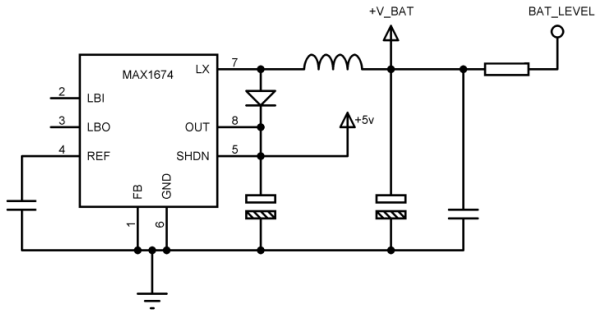


Fig. 2. DC-DC Step-Up Converter.

A mini-USB connector is mounted on the PCB for charging the device. The power lines of the USB port (+V_USB and GND) connect to the on-board IC called LTC4054 (Fig. 3), which regulates the charging current. If the device is connected to another device which only uses the power lines of the USB port, the charging process begins. If it is connected to a computer where data lines (D+ and D-) of the USB port are also present, the dosimeter enters into communication mode, which enables the user to set certain settings and start automatic measurements, logging the results in the computer. Charging also takes place in this mode. Wire called CHARGE is connected to a microcontroller input to indicate charging.

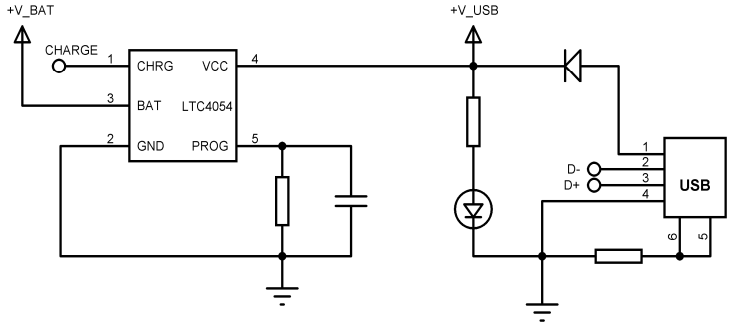


Fig. 3. Charging circuit.

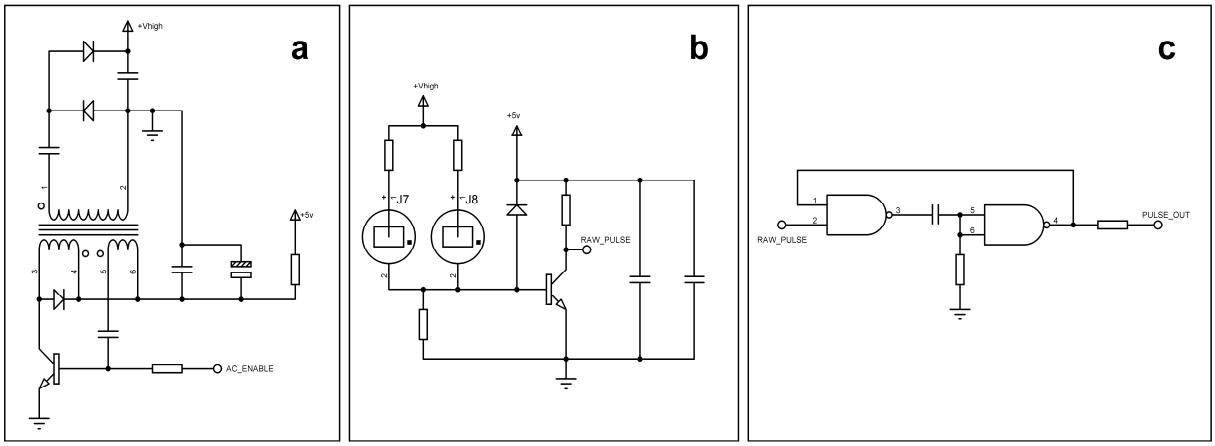


Fig. 4. High voltage generation and detection logic.

The fragment of the circuit presented in Fig. 4(a) is responsible for generating around 350 volts for the tubes. The wire called AC is an output from a microcontroller to enable the high voltage transformer. Whenever logic 1 (5v) is present on the base of the NPN transistor, pulses with a frequency of around 200 kHz occur on the collector, starting high voltage generation. This type of design enables the device to enter sleep mode, which increases the battery life by 70%. The second bipolar transistor (Fig. 4(b)), the base of which is connected to the tubes (J7 and J8), drives the NAND gates [4] that change the state of the PULSE_OUT wire at each event [3]. The NAND gates circuit is presented in Fig. 4(c).

The voltage changes on the tubes have been measured with an oscilloscope and recorded (Fig. 5) during the triggering process. The red line shows the threshold voltage and voltage peaks thatcrossthe threshold border represent particle events.

In this dosimeter circuit, the threshold voltage is around 300mVs. In the following picture, one horizontal grid represents 1 sec., and the vertical grid represents 100mVs. The average pulse width after it has crossed the threshold has been calculated to be around 25 ms.

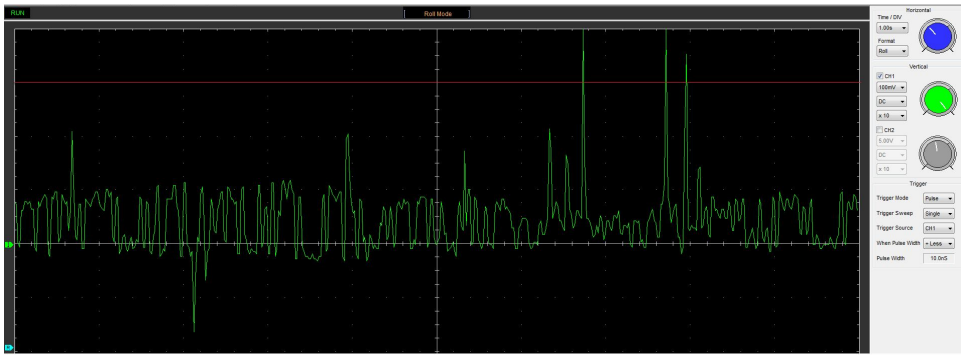


Fig. 5. Tube noise and threshold voltage.

Figure 6 was recorded when the device had been in operation in a higher background radiation.

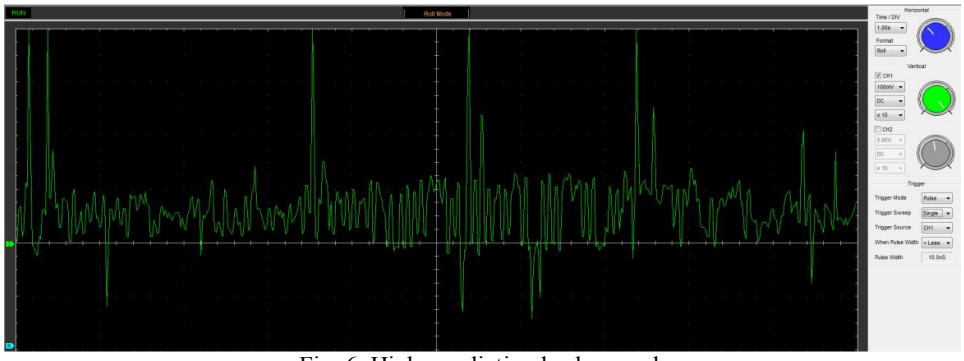


Fig. 6. Higher radiation background.

The full device parameters are presented in the table below.

Table 1. Device parameters

Operating voltage	3.7volts
Maximum in-circuit voltage	350volts
Maximum power consumption	50mA
Power consumption during sleep mode	1mA
Minimum operating temperature	-20º Celsius
Maximum operating temperature	+100º Celsius
Maximum recommended charge cycles	300 cycles
Maximum life for gas filled tubes	5 years
Radiation measurement unit	mR/h
Single measurementtime	20s

The minimum operating temperature is stated as -20ºC, since it is the lowest limit for the LCD present on the device. If the device is operated without an LCD, the minimum operating temperature drops to -35ºC. Measurement error is minimal in the range of 15 ºC - 30 ºC.

The Li-Ion battery capacity drops from around 89%-95% to about 73%-80% after approximately 230 charging cycles. This means that if the device is used continuously, it can last for at least 4 years without the need to replace the battery.

After conducting multiple tests in different environments where the radiation is the same but the temperature varies, it was found that an error of up to 14% can occur in the 10 ºC -35 ºC temperature range. For the purpose of error compensation, an analog temperature sensor (LM95021) has been added to the design. The software has been redesigned to take into account the temperature readings based on which the threshold voltage is shifted with predefined values. Tests show that adding a temperature sensor and error compensation algorithm to the old model cuts down measurement error up to 11%, making the new model as precise as having maximum of 3% error in 10 ºC -35 ºC temperature range. It is important to note, that the error change vs. temperature change graph is nonlinear and a fixed pre-calculated table of error values is hard coded into the microcontroller.

3. Conclusion

The development of the new version of radiation exposure meter presented in this article significantly contributed to the research of particle detection and method development. With the help of this custom-made programmable device it is possible to explore different critical parameters of electronics components used in this design, particularly the temperature depending error occurrence in components. As the error values are not constant and depend on temperature, the new design allows for having more precise measurements with the help of on-board analog temperature sensor. Taking into consideration the pre-calculated error value vs. temperature table, it is possible to design particle detection electronics and measurement equipment in a more reliable manner.

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ELECTRICAL PROPERTIES OF SILICON SURFACE BARRIER A - PARTICLE DETECTORS FABRICATED BY DOPANT DIFFUSION AND VACUUM PULSED LASER DEPOSITION METHODS

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1. Introduction

Currently, the ionization method of recording nuclear particles employs a large number of very different types of detectors from which the solid-state ionization detectors based on semiconductor favorably, because of the high speed drift and life-time of the charged particle formed by the electron-hole pairs, and this is explained by the accuracy of measurement of ionization and significantly higher capacity particle separation with similar energies and virtually instantaneous acquisition and signal processing in a pulse of electric current or voltage.

The development of solid ionization detectors is towards creating inhomogeneous semiconductor detectors (SD) that use properties of the transition between semiconductors with different conductivity type, or between the semiconductor and the metal. Drift, diffuse and surface barrier detectors are the main types of SD used for registration of nuclear radiation. Of these, only surface-barrier detectors have extremely low thickness "dead" layer (~ 0.05 μm), which is very important for the registration of short particles (for example, α - particles). At this stage, for the registration of α - particles are surface-barrier SD based on silicon and cadmium telluride.

Interest in silicon detectors, despite the fact that they are less radiation-resistant than the PDP on cadmium telluride surely retained due to perfectness of technology for obtaining desired quality substrate doping. For example, in [1] the possibility of registration of α-particles (^{238}Pu) with a detector on the basis of surface-barrier structure (SBS) Al-nSi. The procedure for manufacturing the detector comprises the step of chemical etching a silicon substrate surface, followed by a low-resistance thermal deposition of gold and aluminum barrier contact. Earlier we demonstrated the possibility of registration of α - particles on silicon-based SBS by using of a situated close to the surface of p-n junction [2] and heterostructure amorphous carbon (aC)/crystaline Si manufacturing by dopant diffusion and vacuum pulsed laser deposition (PLD) [3] methods, respectively. Both kinds of detectors have a good spectrometric characteristics during registration of α-particles (FWHM α = 22 KeV). The studies of electrical characteristics of this SBS are present in this paper.

2. Experimental detailes

n-type (ρ = 20 Ω.cm) industrial quality silicon (thickness 350 μm) wafers were used as a substrate for fabrication of SBS. Before using there were degreased in pure acetone, washed in redistilled water and dried in air jet. Below is producing technology of SBS.

a) PLD technology of fabrication of Si based SBS.

Si based SBS have been obtained by vacuum (2×10^{-5} mm Hg) laser deposition (1.064 mkm wavelength, 30 ns pulse duration, energy 0.35 J and intensity of ~10^9 W/cm^2 in the target irradiation zone) of amorphous carbon (a-C) film (thickness 100 nm) from the carbon target on n-type Si substrate at room temperature. The thickness of deposited layer from a single laser pulse was determined by dividing of measured on profilometer AMBIOS XP-2 thick layer on a number of laser pulses (0.5 nm per pulse). Low resistance contacts (Ag on a-C и Sb on n-Si) were obtained by PLD after laser deposition of a-C layer. Metalization of low resistance contacts were formed by vacuum thermal deposition of indium.

b) Technology of fabrication of SBS based on Si p-n junction.

Silicon based SBS p-n junction is manufactured in several stages. Initially it is manufactured source for multiple boron diffusion by heat treatment (six-hour annealing at 1200 ^{0}C) powder of boron oxide (B_2O_2). Next, n-type Si substrates were located in the cassette, which is covered on top by cassette with fabricated diffusant (distance between diffusant and substrate - 1 cm), and then introduced into furnace zone at temperature of 1100 ^{0}C. Diffusion annealing lasts for 40 minutes. After diffusion the substrates transported into the solution (H_2O - 3, HNO_3 - 1, H_2SO_3 - 1, HCl - 1) for removal of borosilicate glass. Then the diffusion layer thins by means of grinding. Deposition of metal contacts on the back side of substrate, and on the diffusion layer via a mask is carried out by electrolysis of nickel. Further, annealing of nickel film is performed during 15 min at temperature 700 ^{0}C in vacuum (2×10^{-5} mm Hg). Produced in this manner samples had a depth of p-n junction order of 3 mkm.

Electrical properties of fabricated junctions were studied from measured at room temperature dark ccurrent-voltage (I-U) and capacitance-voltage (C-U) characteristics by using of Keithley-6430 Sub-Femtoamp Remote SourceMeter and capacitance meter E7-25.

3. Results

3.1 Electrical characteristics of SBS based on Si p-n junction

a) C-U characteristics.

Figure 1 shows measured at 1 MHz $1/C^2$ dependence on the voltage for Si p-n junction (- on p-Si). The linearization of dependence C^{-2}-U (capasitance cut-off $U^C_{cut\ off}$ = 0.52 V) indicates the sharpness of impurity distribution in space charge region. The width of space charge region at zero bias voltage on junction is: $W = \varepsilon_{Si}\varepsilon_0 S/C(0) = 1.14$ μm, where $\varepsilon_{Si} = 11.8$, $\varepsilon_0 = 8.85\times10^{-14}$ F/cm, C(0) = 4600 pF. The maximum value of the electric field in the layer of space charge region is: $E_m = 2U^C_{cut\ off}/ W = 9\times10^3$ V/cm. The diffusion potential obtained from the C^{-2}-U data equals to $V_{di} = 0.55$ V ($V_{di} = U^C_{cut\ off} + kT/e$).

b) I-U characteristics.

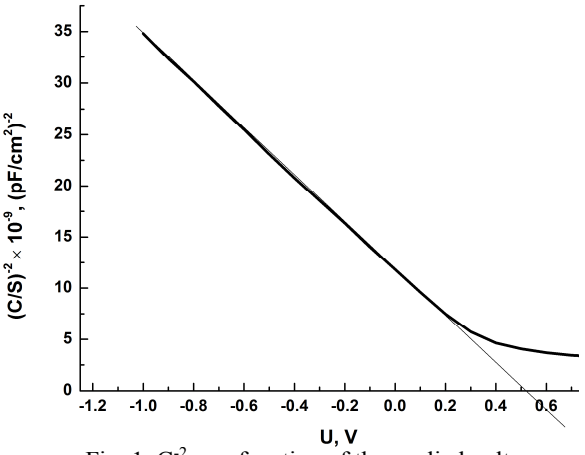

Fig. 1. C^{-2} as a function of the applied voltage.

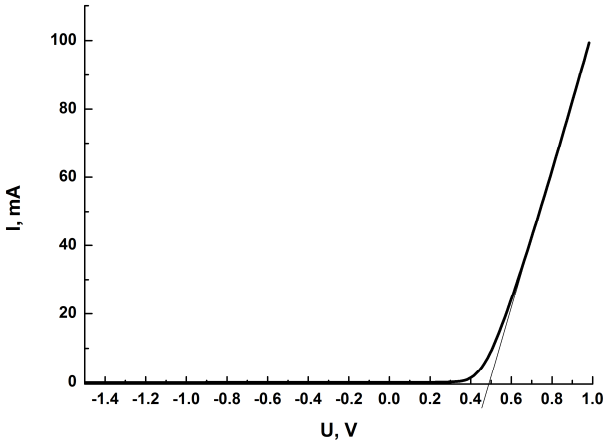

Fig. 2. Dark I-U curve of Si p-n junction.

Figure 2 shows dark I-U curve of Si p-n junction. We have a rectifying junction with rectifying coefficient k (ratio of forward current to reverse) of 1.1×10^3 at 0.6 V bias voltage. Higher than 0.5 V direct current (- on n-Si) is characterized by linear dependence of $I = (U - U^I_{cut\ off})/R_d$, with $U^I_{cut\ off}$ = 0.48 V current cut-off voltage and R_d = 12.7 Ohm residual differential resistance. I-U characteristic of junction at direct biases 0.065 V < U <0.45 V satisfactory fits with the expression for current $I = I_0\exp(eU/nkT)$ at the value of nonideality coefficient n = 2.

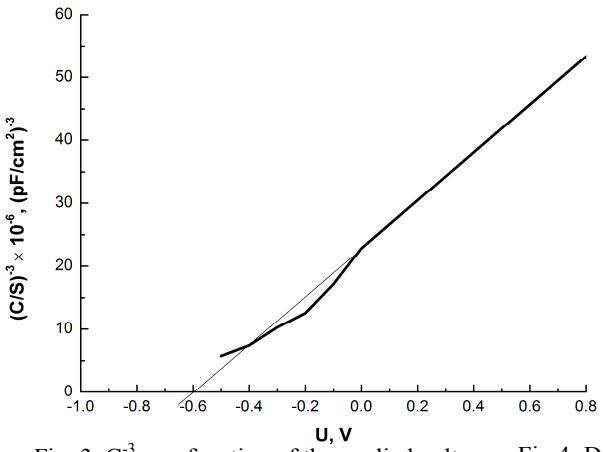

Fig. 3. C^{-3} as a function of the applied voltage.

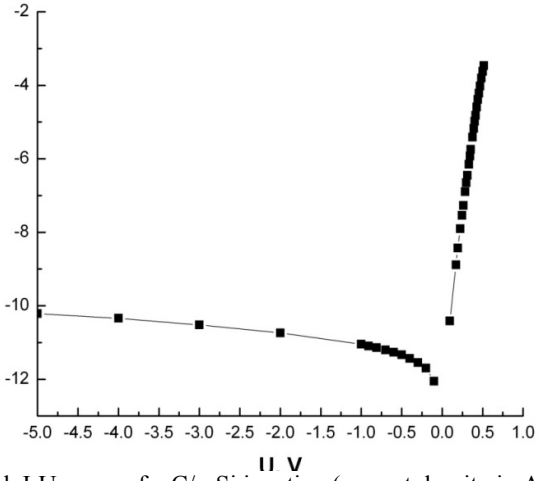

Fig.4. Dark I-U curve of a-C/n-Si junction (current density in A/cm^2).

3.2 Electrical characteristics of SBS based on a-C/n-Si junction

a) C-U characteristics.

Figure 3 shows measured at 1 MHz $1/C^3$ dependence on the voltage for a-C/n-Si junction (+ on n-Si). The linearization of dependence C^{-3}-U (capasitance cut-off $U^C_{cut\ off}$ = 0.6 V) indicates the linearly graded impurity distribution in depletion region of n-Si. The width of space charge region at zero bias voltage on junction is: $W = \varepsilon_{Si}\varepsilon_0 S/C(0) = 1.35$ μm, where ε_{Si} = 11.8, $\varepsilon_0 = 8.85\times10^{-14}$ F/cm, C(0) = 135.7 pF. The maximum value of the electric field in the layer of space charge region is: $E_m = 6.7\times10^3$ V/cm ($E_m = nU^C_{cut\ off}/(n-1)W$, where n=3). The diffusion potential obtained from the C^{-3}-U data equals to V_{di} = 0.63 V ($V_{di} = U^C_{cut\ off} + kT/e$).

b) I-U characteristics.

We have a rectifying junction with $k = 2.2\times10^3$ at 0.5 V bias voltage. Higher than 0.45 V direct current (- on n-Si) is characterized by linear dependence of $I = (U - U^I_{cut\ off})/R_d$, with $U^I_{cut\ off}$ = 0.43 V current cut-off voltage and R_d = 530 Ohm residual differential resistance. I-U characteristic of junction at direct biases 0.15 V < U < 0.45 V satisfactory fits with the expression for current $I = I_0\exp(eU/nkT)$ at the value of nonideality coefficient n = 2.4 (see Fig. 4). Finally the height of barrier calculated from saturation expression $I_0 = A^{**}T^2\exp(-e\Phi_b^I/kT)$, where A**=110 for n-Si, equals to Φ_b^I=0.7 eV.
The table 1 shows the main parameters of obtained structures.

Table 1. Main parameters of obtained structures

Junction	V_{di}, eV	$U^I_{cut\ off}$, V	Φ_b^I, eV	R_d, Ω	n	k	C(0)/S, pF/cm^2
p-n	0.55	0.48		12.7	2	1.1×10^3 at 0.6 V	9200
a-C/n-Si		0.43	0.7	530	2.4	2.2×10^3 at 0.5 V	7800

4. Conclusion

Both kinds of SBS have a non-linear current-voltage characteristics with same order of rectification coefficient, almost the same capacity density, current cut-off voltage and a good spectrometric characteristics during registration of α-particles. PLD method is more manufacturable in terms of technology, as it excludes the processes of implantation, diffusion and annealing.

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GAS, BIO- & CHEMICAL SENSORS

LABEL-FREE SENSING OF BIOMOLECULES BY THEIR INTRINSIC MOLECULAR CHARGE USING FIELD-EFFECT DEVICES

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1. Introduction

The detection of adsorption and binding of biomolecules onto charged surfaces is of great interest for a wide variety of applications, ranging from clinical diagnostics, drug and food industry over biosensors, DNA (deoxyribonucleic acid)-microarray and protein-chip technology up to detection of biowarfare and bioterrorism agents [1-4]. For instance, more than one hundred types of proteins have been recognized as disease markers and can be detected with the traditional enzyme-linked immunosorbent assay. In addition,about 400 diseases are diagnosable by molecular analysis of nucleic acids [5], and this number is increasing daily.

Most of the techniques currently employed for DNA hybridization and protein detection are based on labeling strategies, where different markers (e.g., fluorescence, redox, enzymatic) are used for a signal generation and readout. In spite of their high sensitivity and low detection limit, these techniques suffer from the fact to be time-consuming, expensive and unsuitable for an implementation in portable point-of-care or mobile diagnostic systems [6]. Therefore, the development of tools that could distinguish specific biomolecules without the need for labeling (i.e., label-free biosensing) is of great interest. Label-free biosensors offer enormous potential as clinical diagnostic tools, because of their suitability for real-time and multi-target analysis as well as cost-effective rapid diagnosis. One favorable possibility to detect unlabeled biomolecules is the detection of their intrinsic molecular charge by means of semiconductor field-effect devices (FED) [4, 7-13],since the vast majority of biomolecules are charged under physiological conditions. Label-free electrical detection of charged molecules using different types of FEDs based on an electrolyte-insulator-semiconductor (EIS) system, like electrolyte-gate field-effect transistors, silicon-nanowire transistors, capacitive EIS sensors or light-addressable potentiometric sensors (LAPS), has attracted much attention owing to the well-established semiconductor technologies available for the large-scale production of miniaturized FED-based biosensors, DNA and protein chips. The present paper summarizes recent developments and current research activities in the field of a label-free sensing of biomolecules by their intrinsic molecular charge using FEDs, mainly focusing on the DNA-immobilization and hybridization detection with capacitive EIS sensors and LAPS devices.

2. Functioning principle of capacitive FEDs and mechanism of label-free electrical DNA detection

Most of the DNA-detection methods rely on a DNA-hybridization reaction by which the unknown single-stranded DNA (target ssDNA) is identified by a probe ssDNA, forming a double-stranded DNA (dsDNA) helix structure with two complementary strands. The unique complementary nature of this binding reaction between the base pairs, i.e. adenine-thymine and cytosine-guanine, is the basis for the high specificity of the hybridization reaction (even in the presence of a mixture of many different non-complementary nucleic acids).

Fig. 1ashows a schematic of thecapacitive EIS sensor and LAPS for the detection of DNA immobilization and hybridization, which exemplarily consists of anAl-Si-SiO_2 structure modified with a positively charged weak polyelectrolyte layer of PAH (poly(allylamine hydrochloride)). The measurement setup can be switched between the capacitive EIS- or LAPS-mode measurement.For functioning, a DC gate voltage (V_g) is applied to the structure via a reference electrode so that a depletion layer appears in the semiconductor. Since the FEDs are known as surface-charge sensitive devices,the adsorption or binding of negatively charged DNA molecules on the positively charged gate surface will change the space-charge distribution and depletion capacitance in the semiconductor, resulting in a modulation of the flatband voltage of the FED. To readout the variations of the depletion capacitance, a small AC voltage is applied to the EIS sensor, while the LAPS is illuminated with a modulated light, which induces an AC photocurrent to be measured as the sensor signal.The LAPS measurement is spatially resolved. The measured area on the sensing surface is defined by the area of illumination. In the multi-light LAPS (MLAPS) setup [10], the sensor surface at multiple regions is illuminated in parallel by usingan array of infrared light-emitting diodes (IR-LED) (see Fig. 1a).

Due to the screening of the DNA charge by counter ions in the solution, the electrostatic coupling between the charged DNA molecules and the FED and thus,the DNA-immobilization and hybridization signal strongly depends on the Debye length (~3 nm in 10 mM electrolyte solution) and the distance between the charge of the DNA molecules and the gate surface [4,7].With increasing the ionic strength of the electrolyte, the fraction of DNA charge that remains within the Debye

length from the surface, and thus, can be measured with FEDs, is decreased (see Fig. 1b). Moreover, since the DNA charge is distributed along the molecule length, the DNA-immobilization method and orientation of molecules will have a strong impact on the DNA-hybridization signal [14]. These problems can be overcome via the immobilization of ssDNA molecules preferentially flat to the FED surface as well as by the hybridization detection in a low-ionic strength solution [7,10].

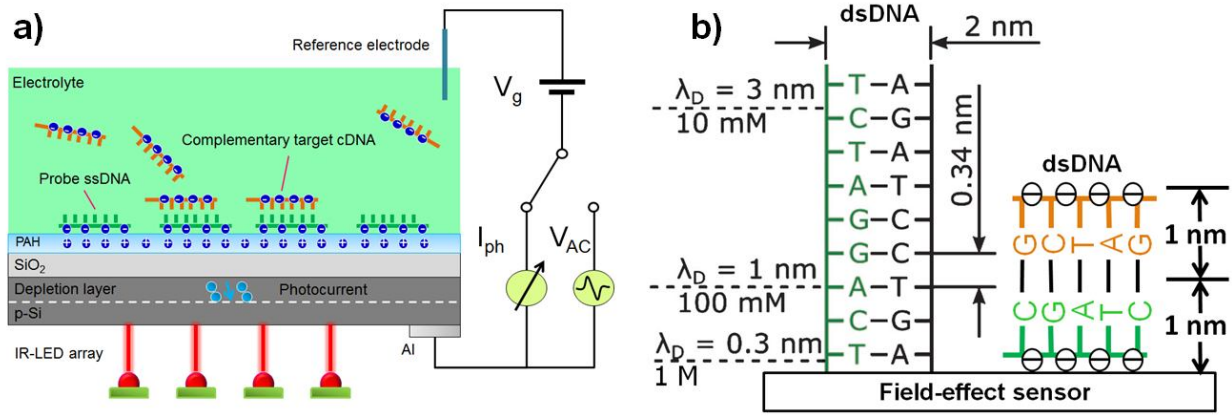

Fig. 1. Schematic of the capacitive EIS sensor and LAPS for the detection of DNA immobilization and hybridization (a) as well as the Debye length (λ_D) and position of DNA charge from the FED surface by different orientations of DNA molecules (b). PAH: poly(allylamine hydrochloride), positively charged weak polyelectrolyte. A: adenine; T: thymine; C: cytosine; G: guanine.

3. Experimental results and discussion

Direct electrostatic immobilization of DNA molecules onto the FED surface is, in general, impossible due to electrostatic repulsion forces between the negatively charged DNA molecules and the FED surface with typically negatively charged gate insulators (e.g., SiO_2, Ta_2O_5, Si_3N_4). In previous experiments, different strategies have been applied for immobilizing probe ssDNA molecules onto the FED surface, like immobilization of thiol-modified ssDNA onto Au surface via gold-thiol bonds or covalent immobilization of amino-modified ssDNA onto silanized SiO_2 surface. Currently, a modification of the sensor surface by means of layer-by-layer (LbL) electrostatic adsorption of a cationic polyelectrolyte/ssDNA bilayer and subsequent hybridization with complementary target cDNA molecules becomes more popular in FED-based DNA biosensors design [10,15,16]. In contrast to often applied covalent immobilization methods that require time-consuming, cost-intensive procedures and complicated chemistry for functionalization of the gate surface and/or probe ssDNA, the LbL adsorption technique is easy, fast, applicable for substrates with any shapes and form [8,17].The LbL-immobilized ssDNA molecules usually form flat elongated structures[18]. As a result, in low-ionic strength solutions, the full DNA charge could probably be positioned near the gate surface within the Debye length, yielding a higher sensor signal.

Fig. 2 demonstrates an example of the DNA-immobilization and hybridization detection with the MLAPS. In this experiment, the normalized photocurrent-voltage (I_{ph}–V_g) curves of the MLAPS were recorded from the single spot (spot 7) before and after consecutive adsorption of a PAH/probe-ssDNA bilayer, and after hybridization of probe ssDNAs with complementary target cDNAs. The normalized I_{ph}-V_g curve of the bare MLAPS has an usual p-type behavior with typical accumulation, depletion and inversion regions. As expected, adsorption of positively charged PAH on a negatively charged SiO_2 surface shifts the original I_{ph}–V_g curve of the bare MLAPS towards the direction of more negative gate voltages, while the adsorptive immobilization of negatively charged probe ssDNAs(20 mer) and subsequent hybridization with complementary target cDNAs (5 µM, 20 mer) results in a shift of the I_{ph}–V_g curves towards the direction of more positive voltages. The direction of these shifts is consistent with the charge sign of the terminating layer. The high potential shifts (averaged over 16 spots) of 83 mV and 32 mV were detected after the probe ssDNA immobilization and target cDNA hybridization, respectively. The density of probe ssDNA and hybridized dsDNA molecules estimated using the measured values of immobilization and hybridization signals were ~5 × 10^{11}ssDNA/cm^2 and ~2 × 10^{11} dsDNA/cm^2, respectively. At the same time, only a small potential shift of less than 5 mV was registered fornon-specific adsorption of fully mismatched ssDNAs. The detection limit evaluated from similar experiments performed using capacitive EIS sensors was ~35 nMcDNA. The results of field-effect experiments with MLAPS and capacitive EIS sensors were supported by contact-angle and fluorescence measurements serving as a reference method to verify the DNA-immobilization and hybridization event.

4. Conclusions

Two kinds of FEDs, namely the MLAPS and capacitive EIS sensor modified with a weak polyelectrolyte PAH layer have successfully been applied for the label-free electrical detection of DNA immobilization and hybridization by their intrinsic molecular charge. To achieve a high immobilization and hybridization signal, the negatively charged probe ssDNA mole-

cules were electrostatically adsorbed onto the positively charged PAH layer using a simple LbL technique. The presence of the positively charged PAH layer enables a preferentially flat orientation of the probe ssDNA and dsDNA molecules near to the gate surface with molecular charges positioned within the Debye length, yielding a higher hybridization signal. The obtained results demonstrate the potential of the MLAPS and capacitive EIS sensor in combination with the simple and rapid LbL immobilization technique as a promising platform for the future development of label-free DNA chips with direct electrical readout.

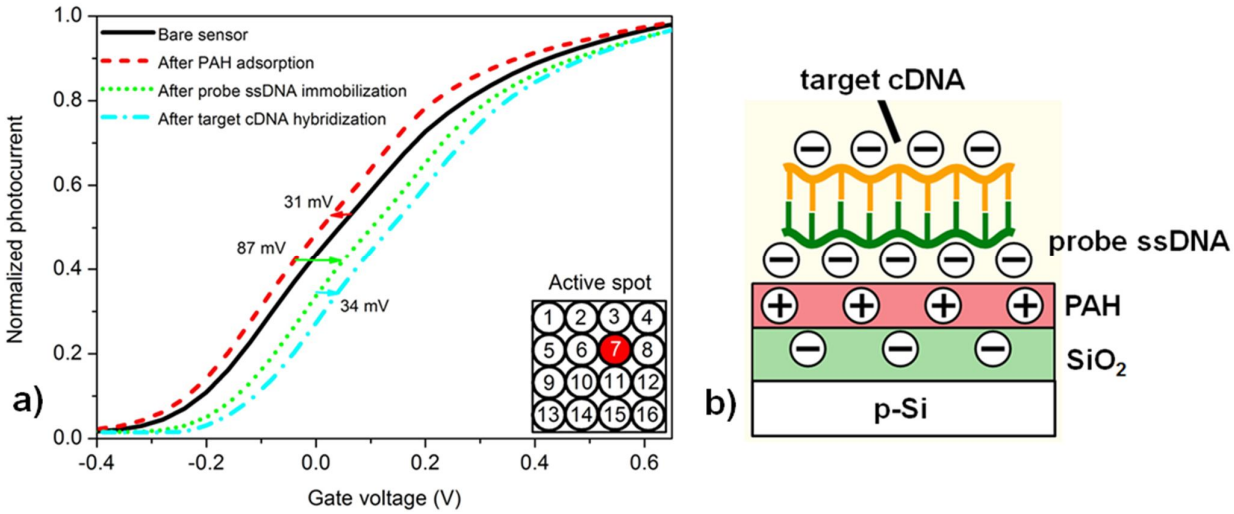

Fig. 2. Typical normalized I_{ph}–V_g curves of the MLAPS recorded from the single spot (spot 7) before and after PAH adsorption, after probe ssDNA immobilization and after hybridization of probe ssDNAs with complementary target DNAs (a) and cross-section of the LAPS structure withthe electrostatically adsorbed PAH, probe ssDNA and target cDNA layers (b). The inset picture shows the spot distribution and position of the measured spot 7.

Acknowledgements

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CHEMIRESISTORS BASED ON Au/Pd NANOPARTICLES AND SILVERPHTHALOCYANINE THIN LAYERS FOR DETECTION OF TAGGANTS IN EXPLOSIVES

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1. Introduction

First artificial phthalocyanine was probably synthesized by accidentin Germany in 1907 [1]. Twenty years later, first phthalocyanine complex with metal (Cu) was created in Switzerland [2]. In 1934, the molecular structure was finally revealed by R. P. Lindstead et al [3,4]. Since that the interest in phthalocyanines is gradually growing as well as the number of their applications [5-7].

Unsubstitued phthalocyanines are extremely stable, insoluble and intensively coloured compounds. Phthalocyanine skeleton is "universal" and can be substituted either with metals (forming metallic complex) or with organic substituents [8,9].

Majority of phthalocyanines are P type semiconductors that are mostly used for detections of oxidizing gases (NO_2, O_3, O_2, Cl_2, …) [10,11]. Semiconductor gas sensors (chemiresistors) form a cheap tool for monitoring of wide spectra of gaseous compounds with redox properties. Monitored compounds exchange electrons with specially designed active layers and thus modulate system's resistance [12].

Nowadays, when the security questions are more and more accentuated, detection of explosives is very topical. Extremely low vapour pressure of explosive compounds makes their direct tracing difficult, therefore majority of detectors are focused on monitoring of accompanying compounds, taggants, also called explosive markers,which are added because of the legal reasons [13-15].

Sensitivity of phthalocyanines towards taggants, i.e. organic nitro compounds is negligible. Therefore, the idea of our approach is to ensure, somehow, the decay (photodecomposition) of taggant molecules leading to NO_2 release.Released NO_2(contrary to organic nitro compounds) can be registeredwithphthalocyanine sensors. Baseda thorough search in literature, the wavelength of 266 nmwas selected to perform the described photodecomposition [16-23].

2. Experiment

The chemiresistors used for detection contained graduated active layers based on Au, Pd and AgPc. Au and Pd nanoparticles are employed as structured base for the thin AgPc active layer. The structured sensor is depicted in the Fig.1.

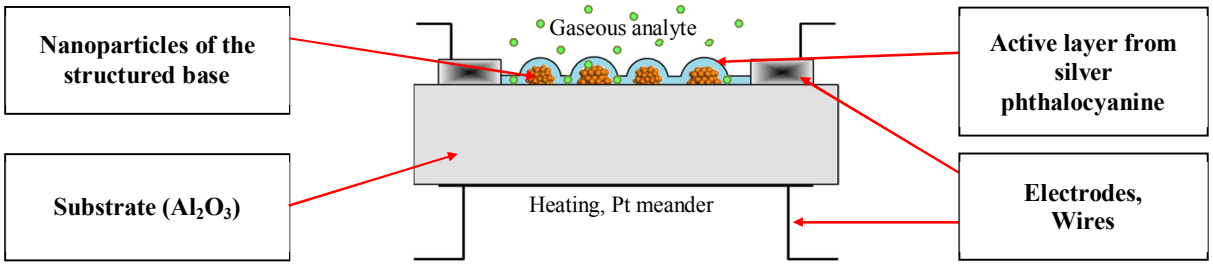

Fig.1. Scheme of nanostructured chemiresistor.

Metallic nanostructures on the alumina (Al_2O_3) substrate were prepared by combination of DC magnetron sputtering (Denton Vacuum Desk V HP TSC, voltage 400 V) with external thermal annealing. Conditions of the sputtering process were as follows – argon pressure 0.73 Pa and sputtering current 4 mA. The target to substratedistance was 30 mm.

Annealing or tempering of the sensor (mostly 400 °C) was provided by integrated Pt meander, powered with programmable current source MOTECH LPS 304. Sensor resistance was in-situ monitored with Agilent 34410A during the sputtering process to prevent formation of continual layer of metal and hence short-circuit.

Formation of metallic nanoparticles was inspected using scanning electron microscopy (VEGA3 TESCAN). Silver phthalocyanine sensing layers were prepared by Organic Molecular Evaporation (OME) method under high vacuum conditions. The evaporation conditions were: temperature of phthalocyanine sublimation source 400 °C, working pressure ≈ 10^{-4} Pa and source to substrate distance 180 mm.

The thicknesses of both metallic and AgPc layers were measured with Quartz Crystal Microbalance (QCM SQM-160, QCM SQM-180). A complementary study of properties of Au and Pd nanoparticles is included. Physical properties of created structures were characterized by conductivity measurements, extensive SEM imaging and UV-VIS spectroscopy.
Preparation conditions of Au and Pd nanoparticles (amount of metal, substrate temperature) were optimized to obtain homogenous nanoparticles with an equivalent diameter in order of hundreds of nanometres for the graduated sensing layers. Impedance spectra were measured for graduated sensors (Agilent 4294A).
The experimentswere also focused on exposition of vapours of various nitro compounds to UV light. UV light was generated in a commercially available mercury lamp and in a Q-switched pulsed laser Nd-YAG (266 nm, 4 ns pulses, 10 Hz, 0.4 J/cm^2). Products of photoreactions were analysed by either quadrupole mass spectrometer GSD320C in range 0–300 amu or by prepared chemiresistors.

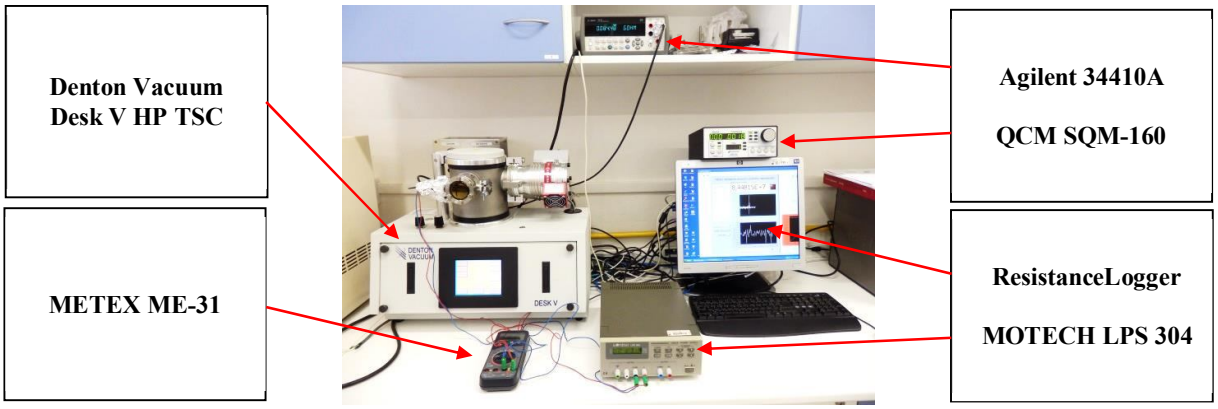

Fig. 2. Sputtering apparatus with in-situ monitoring of electrical resistance and temperature.

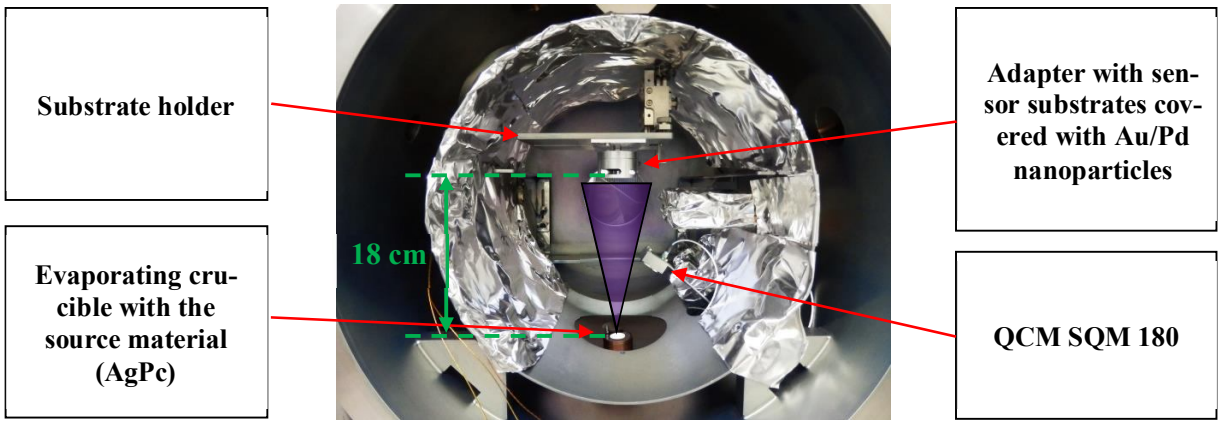

Fig. 3. Chamber of OME system for depositions of active layers onto structured base (Au/Pd nanoparticles).

3. Conclusions

Chemiresistors with graduated sensing layers exhibited excellent sensitivity towards nitrogen dioxide (their resistance decreased approx. 10x for concentration of 2 ppm, Fig. 4). Prepared sensors were insensitive to vapours of water (most common interferent).
Equivalent electrical circuits of the sensors were found. The best fits of measured impedance data were obtained with two or three parallel RC circuits in series.Resistance of graduated sensors was increasing with decreasing temperature and decreasing with increasing absolute value of bias used during the measurement.
Measured massspectra confirmed that UV laser light interacts with vapours of nitro compounds and induce their decomposition towards simpler molecules (Fig. 5).
Nevertheless, the resolution of NO_2 formed during the UV expositionby means of mass spectrometry is very difficult. On the contrary, the presence of NO_2 was easily monitored by prepared sensors with graduated active layers (Fig. 6). The sensitivity (response) was very promising, it equals to 373x towards 150 ppm of irradiated 2-nitrotoluene vapours.
To conclude, this contribution employs photo-induced decomposition of nitro compounds for their indirect detection by means of NO_2 sensors. The created methodology has a potential to detect nitro compounds which are used as markers of

explosives (2-nitrotoluene, 4-nitrotoluene, 2,4-dinitrotoluene, 2,3-dimethyl-2,3-dinitrobutane, ...) in concentrations as low as tens of ppb. Application of NO_2 sensors instead of expensive analytical equipment (ion mobility spectrometers, gas chromatographs …) promises significantcost savings in detections of explosives.

Moreover, metal nanoparticles are used to decrease electrical resistance (up to 100x) of sensors based on phthalocyanines. This reduces the requirements for the level of attached ohmmeter device and as a result it contributes to another reduction of costs.

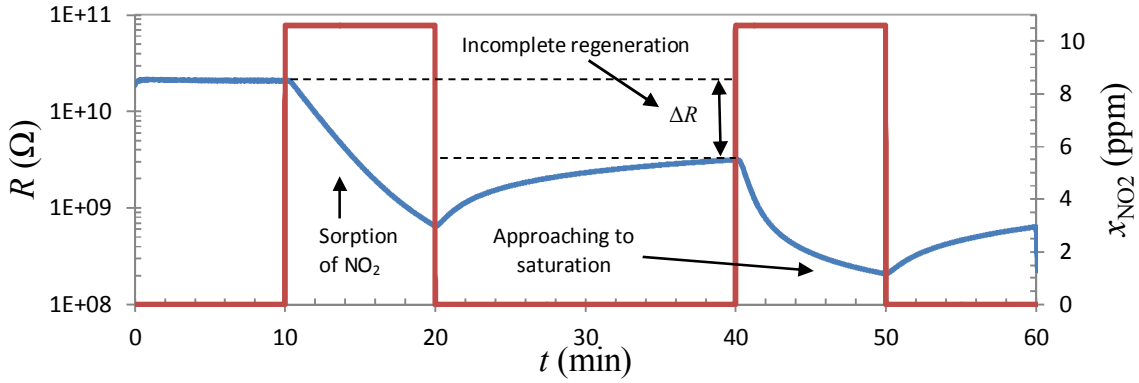

Fig. 4. Detection of 10.6 ppm NO_2 by graduated sensor (50 nm Pd, 50 nm AgPc), 2 cycles, temperature 40 °C.

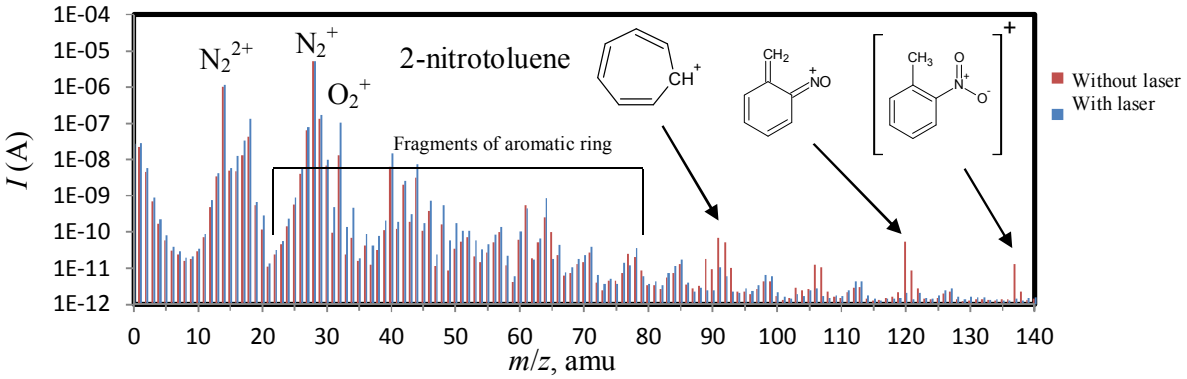

Fig. 5. Spectra's comparison of UV exposed (blue) and not exposed (red) 2-nitrotoluene vapours (150 ppm).

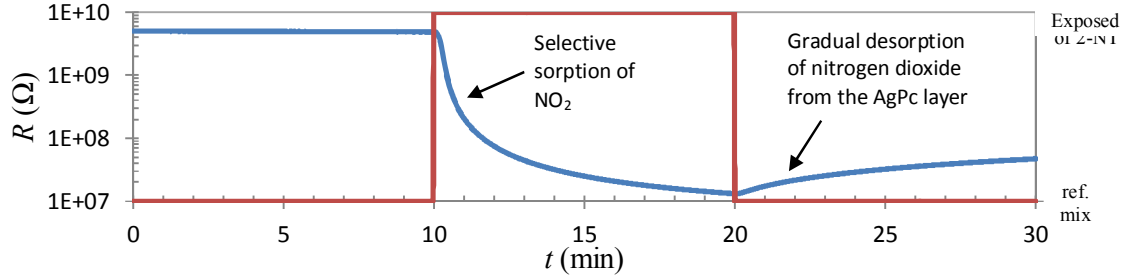

Fig. 6. Detection of NO_2 in saturated vapours of 2-nitrotoluene (25 °C) exposed by light from Nd-YAG laser.

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LOW-FREQUENCY NOISES AND SNR OF DOUBLE GATED Si NW ISFET BASED BIOCHEMICAL SENSOR

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1. Introduction

Sensing chemical and biological species are essential in many areas such as diagnostics of diseases, screening and development of new drugs or environmental monitoring. Ion-sensitive field-effect transistors (ISFETs) based on silicon nanowires (Si NW) have attracted substantial interest for various chemical and biochemical sensing applications yet there remains uncertainty concerning their response to changes in the supporting electrolyte concentration [1-4]. Over the past decades, interfaces between oxides and electrolytes have received considerable attention in different scientific communities. Detection and quantitation of biological species are central to many areas in healthcare. On the other hand signal-to-noise ratio (SNR) is the key metric describing of the sensor performance. In the case of ISFET sensors, the signal (response) is given by a change in surface potential or source-drain currentupon changing the bulk concentration of the targeted analyte. The low-frequency noise ultimately limits the resolution of the sensor. Apart from the pH-response, the evaluation of noise is also an important issue, as it ultimately defines the detection limit of a sensor. Recently, intense attempts have been made to understand the factors determining the SNR ratio [4], however with inconsistent conclusions about the optimal regime for sensing. Noise spectroscopy and transconductance measurements to establish the optimal regimes of operation for Si NW FETs sensors employed in [5]. A strong coupling between the liquid gate and back gate has been revealed and used for optimization of SNR in sub-threshold as well as above-threshold regimes. Liquid-gated Si NW FETs fabrication technique and their transport and dynamic properties are investigated experimentally and theoretically in [6].In this work we investigate current-voltage characteristics (CVC), low-frequency noises, pH-sensitivity and SNR of liquid and back double gated Si NW sensors.

2. Experimental details and results

CVC, low-frequency noise behavior, pH-sensitivity and signal to noise ratio of the front oxide layer (FOX)-p/Si NW-buried oxide layer (BOX)-p/Si substrate structures based double gated p-Si FETsare investigated. Structures are made by the SOITEC- technology (Fig. 1). Thicknesses of the layers are: $t_{FOX} = 9$ nm, $t_{BOX} = 145$ nm, $t_{NW} = 250$ nm, length of the NWis equal to 20 μm. Device has 12 parallel NWs, which manufacturing technique is presented in [5]. The concentration of acceptors in both substrate and NW is 10^{15} cm^{-3} and in p^{+}source and drain regions is 10^{19} cm^{-3}. All 12 parallel NWs are identical. Current-voltage characteristics and spectral density of the low-frequency noise measurements is carried out on one NW at the room temperature.Noise spectral density is measured in the frequency range 2-300 Hz at the several values of the electrolyte pH and liquid-gated voltage. For noise measurements we use standard technique (see e.g. [7]).

Measurements of CVC are performed in an aqueous solution with pH=7. Source-drain current almost does not depend on the pH value. It is shown on Fig. 2. Dependencies of the source-drain current vs. liquid-gate voltage at the several pH and at the back gate off and $V_{DS} = -1$ V is present on Fig. 3. Source-drain current has similar behavior as in [5, 6] and grows at the increasing of the pH value. Such behavior can be explained as follows. As it is well known energetic band gap of the semiconductor is bending in the interfacial area and a depletion region is formed. Width of this region is equal to

$$L = \sqrt{\frac{2\varepsilon\varepsilon_0(\chi_{ox}-\chi_{Si})}{e^2 p}}. \quad (1)$$

Here ε and ε_0 are the silicon and free space permittivity, correspondingly, χ_{ox} and χ_{Si} are affinity energies of the oxide (SiO_2) and silicon, correspondingly, and p is the majority carriers concentration in silicon. Take into account that all shallow acceptors in p-Si NW are ionized at the room temperature we can assume that $p = N_A = 10^{15}$ cm^{-3}. Then we receive $L = 2$ μm that in one order larger than NW thickness. Then we can consider that current channel in p- Si NW completely is depleted and has high resistance. At the $V_{FG} = 0$ V channel is closed and current is absent and with grown of the $V_{FG}(V_{FG} < 0)$ channel began opened and source drain current is increase.Source-drain current is the signal current by means of which we can receive information about sensitivity of electrolyte composition and containing charged ions (pH). The level of the useful signal limited by the internal noises, and particularly by the low-frequency noises since adsorption-desorption processes on the interface electrolyte-oxide is very slow. The measured data is in good agreement with the trap state model, assuming trapping/detrapping of trap states at the Si NW/SiO_2 interface as the one of the sources of the noise.

On Fig. 4 the spectral dependency of the low-frequency noises at the several values of the liquid gate voltage at the 300 K are presented. As it is known in the electrolyte-insulator-semiconductor structures' noises can be formed also by the random tunneling of the majority carriers from the channel to electrolyte. Probability of the tunneling occur when potential

barrier height (in our case front oxide thickness, 9 nm) less or equal to de Broglie wavelength of the majority carriers (in Si it is equal to ~5 nm [8]). Then the tunneling probability is very slow. In this case for description of low-frequency noise we can use correlated number-mobility fluctuation unified $\Delta n - \Delta\mu$ model. According this model the flicker noise spectral density can be presented as follows [9]:

$$S_{V_{DS}}(f) = \frac{e^2 kT}{\gamma f W L C_{ox}^2}(1 + \alpha\mu_h p)^2 N_t(E_f). \quad (2)$$

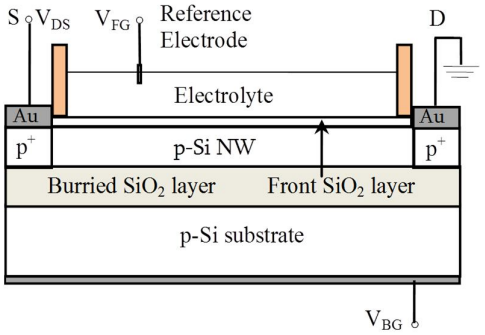

Fig. 1. Schematic presentation of Si NW FET with liquid and back gates.S and D indicate source and drain. V_{DS} is the source-drain voltage, V_{FG} and V_{BG} are the liquid and the back gate voltages, correspondingly.

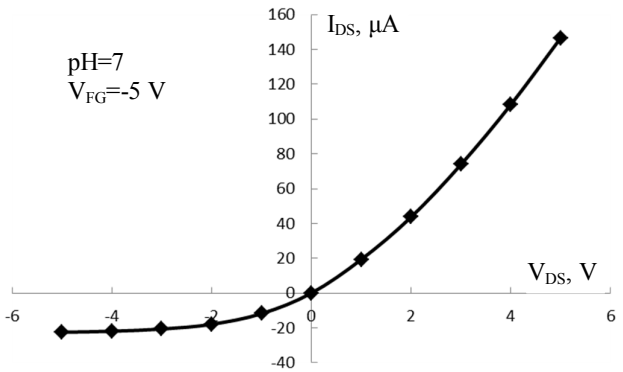

Fig. 2. Source-drain CVC at the V_{FG}=-1V, V_{BG}=0V and pH=7.

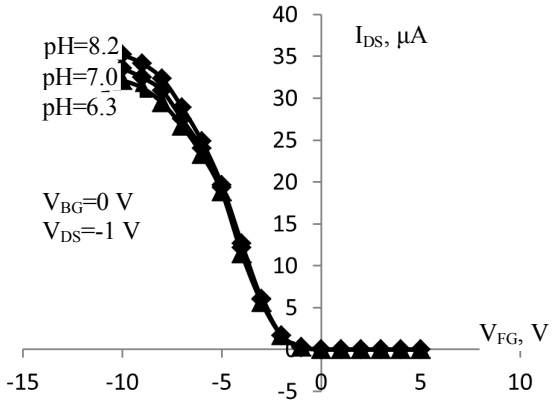

Fig. 3. Dependencies of source-drain current vs liquid gate oltage at the several pH values.

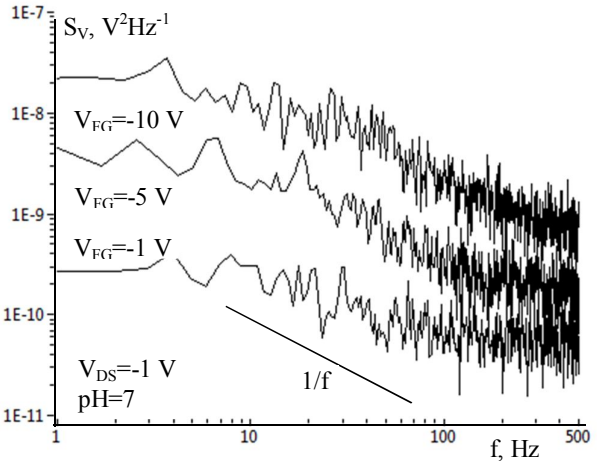

Fig. 4.Noise spectral density at the several values V_{FG}.

Here W and L are the channel width and length, correspondingly, C_{ox} is the capacitance of the insulator layer (SiO_2), $\gamma = 4\pi\sqrt{2m_{ox}^*\phi_B}/h$ is the tunneling parameter (for Si-Si0$_2$it equals 10^8 cm^{-1} [10]), ϕ_B is the tunneling barrier height for the electrons at the interface,m_{ox}^* is the electron effective mass in the oxide, $\alpha = \pi m^* e^2/4hkT(\varepsilon_{Si} + \varepsilon_{ox})^2$ is the carriers density function formed by reason of screening effect, m^* is the electron effective mass in the silicon,μ_h is the holes mobility,$N_t(E_f)$ energetic distribution of the traps, E_f is the Fermi energy. As it is follows from Eq. (2) $S_{V_{DS}} \propto p^2$. In favour of application unified $\Delta n - \Delta\mu$ model for description of the noises indicate curve in Fig. 5, where dependency of the normalized noises vs. majority carriers concentration is presented. This dependency also follows as quadratic dependence. Values of the p calculated from linear part of CVC [9]:

$$I_{DS} = \frac{ep\mu_h W V_{DS}}{L}. \quad (3)$$

As it is known pH-sensitivity usually isdetermined by the changing of the semiconductor surface potential, which directly influences on the I_{DS} changing. Then pH-sensitivity R_{pH} can be determined also as follows:

$$R_{pH} = \frac{\Delta I_{DS}}{\Delta pH}. \quad (4)$$

As it is shown on Fig. 6, pH-sensitivity increases with increasing of the liquid gate voltage and can reach up to several μA. At the high values of the V_{FG} sensitivity is saturated,as at the higher values of the V_{FG} almost all carriers in the channel will take part in the source-drain current.

In Fig. 7 dependencies of the signal to noise ratio depending on liquid gate voltage are presented at the several frequencies. It is calculated according to following expression [5]:

$$SNR = \frac{\Delta V_{FG_{Signal}}}{\sqrt{S_V \Delta f}}. \quad (5)$$

Here $\Delta V_{FG_{Signal}}$ is the signal value of the liquid gate voltage and $\Delta f = 1$ Hz is the frequency unit interval. For numerical calculation we take $\Delta V_{FG_{Signal}} = 1$ V. At the low values of theliquid gate voltages SNR can reach up to very high values $\sim 10^5$.

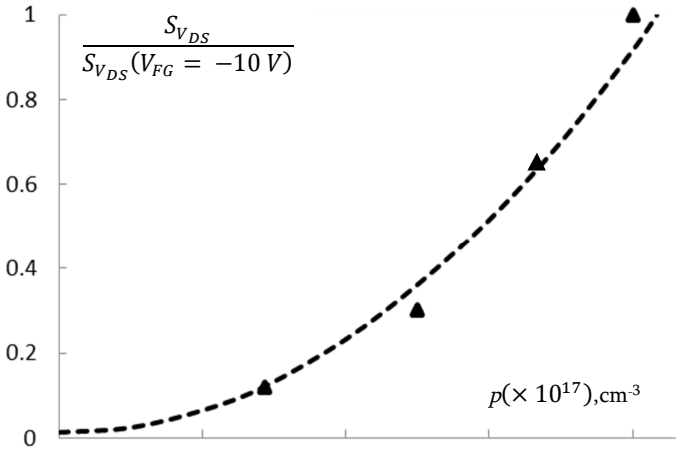

Fig. 5. Normalized noise dependency vs. carrier's concentration.

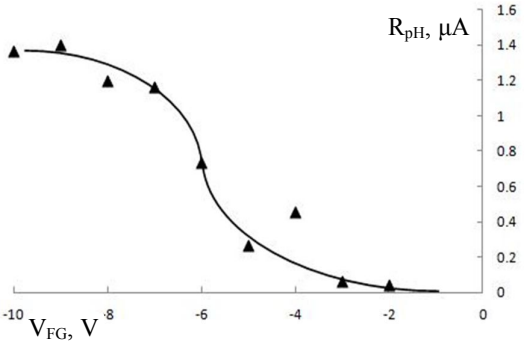

Fig. 6. Dependencies of pH-sensitivity from liquid gate voltage.

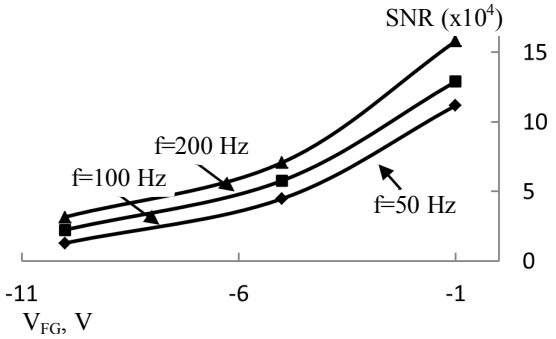

Fig. 7. Dependencies of SNR from liquid gate voltage at the several frequencies. Gate signal voltage $\Delta V_{FG,\ Signal}$=1 V.

3. Conclusion

CVC, low-frequency noises, pH-sensitivity and SNR for liquid and back double gated Si NW sensors are investigated. It is shown that source-drain current substantially depends on pH-value and grows with increasing of the liquid gate voltage. Low-frequency noises level increases and noise index decreases from 1.1 to 0.7 at the growth of V_{FG} value. Noises' behavior is successfully explained in framework of the correlated number-mobility fluctuation unified model. Using noise spectroscopy it can be determined majority carriers concentration in the nanosized channel. pH-sensitivity increasesas a result of the liquid gate voltage increase, giving opportunity to measure very low proton concentrations in the electrolyte medium at the high values of the V_{FG}. SNR for Si NW based biochemical sensor has higher value, reaching up to 10^5.

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DECORATED CARBON NANOTUBE SENSORS

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Carbon nanotubes (CNTs) have been studied extensively and have opened a new science and technology field on nanoscale materials. CNTs are one-dimensional materials; they show many interesting effects and properties. CNTs are graphene sheets of covalently bonded carbon molecules rolled into hollow cylinders. There are two main types of CNTs: single-walled nanotubes (SWCNTs) which have a single carbon layer with a diameter of 1–5 nm and multi-walled nanotubes (MWCNTs) which have multiple layers of carbon (with an interlayer spacing of 0.34 nm), that are concentrically nested together. Multi-walled nanotubes have outer diameters as small as 5.5 nm and inner diameters as small as 2.3 nm. Essentially, CNTs are one-dimensional materials-quantum wires. They have been studied extensively and shown various kinds of size effects in their structures and properties. CNTs demonstrated unique mix of electrical, optical, thermal and mechanical properties. The potential of applications of CNTs is shown in nanoelectronics, sensors, displays, hydrogen storage, batteries etc. A strong demand of cheap, high-sensitive and selective gas sensors involves domestic safety, homeland security, quality control, environmental monitoring et al. The development of CNT based gas sensors and sensor arrays has attracted intensive research interest in the last years because of their potential for the selective and rapid detection of various gaseous species by novel nanostructures integrated in miniature and low-power consuming electronics. More often, the easy CNT configurations as chemiresistors and chemical field effect transistors are used as nanosensors. In these sensors, the electrical properties of nanostructures are dramatically changed when exposed to the target gas analytes. When electron-withdrawing molecules (e.g. NO_2, O_2) or electron-donating molecules (e.g. NH_3) interact with the p-type semiconducting CNTs, they will change the density of holes in the nanotube, which changes the conductance of CNTs. This creates the basis for applications of CNTs as electrical chemical gas sensors. The range of molecules detected by SWCNTs is very limited due to large binding energies and charge transfers with the nanotubes. Some gases (CO, O_2, N_2, and CO_2) and water, for example, do not physicosorb, do not influence on the intrinsic electron spectra and cannot be detected by SWCNTs. For the case of NO_2 and NH_3, they can be physicosorb on the SWCNT surface even at room temperature. Even under high vacuum, the desorption of many gases is too slow for sensor applications, it is necessary to dramatically increase the pre-heating temperature of the work body of the sensor (up to 700K). So, regretfully, gas sensor made of pristine SWCNT has such limitations as low adsorption energy, affinity or long recovery time.

These shortcomings can be, at least in part, circumvented by a CNTs decoration. There are the following approaches for the surface functionalization of CNTs by organic materials, doping of CNTs, by catalytic metal nanoparticle/nanocluster as well as metal oxides. Such approached are discussed below.

CNT gas sensors functionalized with organic polymers

Organic polymers in gas sensors react to analytes by changing their physical or chemical properties. Among such polymers having delocalized bonds that make its semiconducting or even highly conductive, polyaniline, polypyrrole, and polythiophene should be mentioned. Amperometric, voltammetric, conductometric and potentiometri sensors of ammonia, nitrogen dioxide, carbon monoxide and VOCs made from such polymers. The conductance changes observed due to modulating the doping level in the conducting polymers upon exposure to analytes. It was showed that non-covalently drop coating of polyethylene mine (PEI) and Nation (a polymeric per fluorinated sulfuric acid monomer) onto SWCNT. ChemFETs resulted in gas sensors with improved sensitivity and selectivity for NO_2 and NH_3. SWCNTs from p-type to n-type semiconductors were able to detect less than 1 ppb NO_2 while being insensitive toward NH_3. In contrast to PEI-coated sensors, Nafion coated SWCNTs were insensitive to NO_2 while exhibiting a good sensitivity toward NH_3. PEI–polymer-coated SWCNT ChemFETs had n-type characteristics and were used as CO_2 gas sensors having a high sensitivity, fast response time and complete reversibility for CO_2 concentrations ranging from 500 ppm to 10% in air. The SWCNT-Ethyl cellulose and polymethylmethacrylate sensors are reported, chlorosulfonated polyethylene and hydroxypropyl cellulose are used for detection of Cl2 and HCl. NH_3 sensor made of composite PVP polymer and CNT film shown rather fast response, which did not detected for CNT sensor. Polymer coated SWCNT sensors for detection of dimethyl methylphosphonate were also realized. Synergistic effect in the oxygen and NH_3 gas sensitivity of polypyrrole/SWCNT composites were demonstrated. The modification in polypyrrole results in a synenergistic effect – nanocomposite has ten times more sensitive than sensors made of polypyrrole or SWCNT separately.

Metal nanoparticle/nanocluster functionalized CNT gas sensors

Elemental Pd and Pt are well-known catalysts with high H_2 solubility and diffusivity, as well as good corrosion resistivity. Pd-functionalized SWCNTs shown high sensitivity toward H_2, with a 50% greater sensitivity of up to 50% relative resistance change to 400 ppm H_2 for individual Pd-functionalized SWNTs compared to SWCNT bundles. The response time was 5– 10 s, and the time for recovery was about 400 s. The adsorbed H_2 molecules are dissociated as hydrogen atoms, which dissolve into Pd with a high solubility, leading to a decrease in the work function of Pd. This increases electron transfer from Pd to SWNT and causes a decrease in conductance. The process is reversible.

Gold has been found to be sensitive to odorous gases containing thiol vapor and H_2S. Single wall and multiwall CNTs decorated with different metals (Rh, Ni, Au, Pd, Al, Ag etc.) were proposed for detecting H_2S, CH_4, H_2, CO, O_3, C_6H_6, NO_2, CO_2, CH_4, C_2H_5OH and NH_3. CNTs with comb electrodes can be used to detect gases at low concentrations (e.g. low ppb level). CNTs films coated by Co-catalyst perform chemical detection of NO_2, NH_3, CO_2, CH_4, CO and C_2H_5OH are operated at room temperature. Compared to polymer-based sensors, metal-based sensors are mechanically and chemically robust and stable, and can operate at higher temperatures and in harsher environments.

Review of previous papers

Some thin or thick films of metal oxides show a fast response to varying gas atmospheres, and they are appropriate for gas sensing systems. Different gas, smoke and ion-selective sensors were investigated and developed by us at Yerevan State University. Gas sensors were made from Bi_2O_3, SnO_2, ZnO, TiO_2, In_2O_3, Ga_2O_3, Fe_2O_3 thin films and other ceramic materials as well as porous silicon. Earlier we developed their theoretical basis and realized gas sensors practically without pre-heating of work body of the sensor. For example, in the case of sensors made of Bi_2O_3, $NaBiTi_2O_6$, $LaAlO_3$-$CaTiO_3$, $Fe_2O_3$and $Bi_2V_4O_{11}$, operating temperature was equal to 20-70^oC. Such sensors were sensitive to smoke, ethanol and sulphur vapors as well as to humidity. Our Bi_2O_3 smoke detectors are competitive with photoelectric (optical) and ionization detectors of smoke, which currently can be widely used in fire-alarm systems. Independent testing of our adsorptive type smoke detectors in the USA yielded promising results. We also investigated different metal oxide photoelectrodes for photo-electrochemical conversion of solar energy.

There are several commercial products now, especially made of tin dioxide. These types of sensors continue to suffer of high pre-heating temperature of work body of the sensor, i. e. high consumption of energy, lack of selectivity and long-term stability which limits their applications. Usually SnO_2 sensors do not perform well at room temperature. The range of their operating temperatures spans from 200 to 500 °C. For example, the sensor for O_3 gas showed the most effective at 350°C. Many commercial SnO_2-based sensor devices have been realized to detect organic compounds and hazardous gases (e.g., CO and NO). These gas sensors often operate at high temperatures up to 400°C. Note that existing platinum wire sensors need also in its heating above 400°C and very high cost.

The main problem today is to develop new semiconductor gas sensors working at or near room temperature of work body. In addition, they should be small, cheap and easy to be inserted into microelectronic integral circuits. We report below shortly results of our investigations of metal oxide and CNT sensors were carried out recently with the aim to decrease the temperature of their work body. Physical and gas-sensing behavior of semiconductor sensors depends directly on their preparation methods and conditions. One of the main objectives for research at YSU is to develop nanoparticles, because decreasing in the particle size raises the effective surface area for gas adsorption. The nanosized particles, porosity of the films, and the large surface/ volume ratio ensure high sensitivity. Below a certain critical nano-crystallite size, the sensitivity of the gas sensor increases sharply. This occurs when the nano-crystallite size becomes comparable with the double space-charge layer thickness of the semiconductors under consideration. For nano-crystalline SnO_2 thin film or powder, the calculated value of the space-charge layer thickness is ≈ 3 nm. Our efforts were mainly focused on developing and improving the nanocrystalline SnO_2 processing technique. We studied the response of sensors to detect the presence of H_2 in air at various temperatures (25-300^{0}C). As a result, the maximal response is registered in the 80-130^{0}C range of operating temperatures; although rather high sensitivity to H_2 gas at room temperatures was observed.

Gas sensors made from metal oxides doped with metal cations

Several studies have been focused on doping the SnO_2 matrix to increase the sensitivity of the resulting sensors. Introduction of transitional metal cations into an oxide matrix leads to an increase in surface states, active sites and free carriers, which is important for gas sensor application. For example, the addition of Nb into TiO_2 enhanced the response to CO as it induces the formation of new electronic states, due to its donor-type behavior. Vanadium doped with tin dioxides has a higher response towards SO_2 gas, because of their redox activity for SO_2 oxidation to SO_3. Doping with CuO, MoO_3 and Fe_2O_3 leads to lowering of the work body pre-heating temperature of a sensor and increasing in gas response. Vanadium cations serve as reducible catalytic centers to promote oxidation reactions and enhance O_2 consumption. It is known also that dispersed V–O-support structure adsorbs CO gas at ambient temperature.

Metal oxide-CNT gas sensors

Gas sensors can be realized on the base of SnO_2/CNTs, TiO_2/CNTs, Fe_2O_3/ CNT, WO_3/CNT and Co_3O_4/CNT composites. Using mixed SnO_2 nanoparticles with 1 wt. % MWCNTs (100:1) sensing materials, gas sensors were fabricated on micro-platforms made of thick SiN_x membrane. The sensing materials were prepared by mixing SnO_2 nanoparticles and MWCNTs with polymer vehicles to form paste. Such sensors were characterized to NO_2, NH_3 and xylene gases, respectively, as a function of temperature from 180°C to 380°C. It was found that 220°C was the optimum temperature to have the best sensitivities.

We used a MWCNT membrane prepared at Yerevan State and/or Szeged (Hungary) Universities for the manufacture of the nanocomposite SnO_2/MWCNT thin film gas sensors by the sol–gel method. Surface modification of the CNTs/metal-oxide hybrid gas sensors with noble metals (Pt, Pd, Au, Ru, and Rh) promotes an improvement of the gas sensors sensitivity and selectivity because of these metals or its oxides are the catalysts for chemical reactions taking place on the surface. The increase in the electrons concentration in the semiconductor conduction band leads to the reduction of structure resistance in the case of the detection of reducing gases.

It is known also that ruthenium stimulates an increase in the rate of oxidation and other surface reactions, involving adsorption of oxygen from the air on the structure surface which causes an increase in the depletion layer of semiconductor near-surface region and hence leads to the enhancement of the sensor response. Our investigations have shown that high response appears only after sensibilization of the MWCNT/SnO_2 tablets in 0.01 and 0.03 $Ru(OH)Cl_3$ water solution. Changes in the sensor resistance were registered at operating temperature 100-350°C. For example, sensors made of the MWCNT/SnO_2/Pd tablets sensitized with 0.03 M Ru (OH) Cl3 solution during 20 min demonstrated rather high response to hydrogen and isobutane already at 120 °C. The resistance of the sensor work body (~700 kOhm) decreased 10 times in ~10 and ~30 s after the injection of isobutane and hydrogen, respectively. Unfortunately, sensors recovered rather badly at this temperature. The recovery time for this sensor was equal ~30 and 15 min after a loss of, respectively, isobutane and hydrogen supply at 120 °C.

Gas i-butane is widely used for domestic purposes, in the cooling plant, and as a fuel, being a part of LPG. Vapors of this gas are hazardous to the human health. Therefore the detection of isobutene vapors in the environment is an important problem. Note that we did not detect i-butane by our sensors made of pure SnO_2 and pure CNTs. But we convinced that the response and selectivity of sensors made of a nanocomposite consisting both non-functionalized CNT and inorganic nanoparticle like SnO_2, ZnO or another metal oxide are dramatically increased. In such hybrid sensors we realized some synenergistic results. The measurements of the sensor response to isobutane at higher temperatures have shown that characteristics become more stable. The sensor reaches the equilibrium state faster, the recovery time decreases down to ~10 min. The sensor response increases with the increase in temperature. The sensors made of the MWCNT/SnO2 nanocomposite sensitized with the 0.03 M Ru (OH) Cl3 solution were the most sensitive ones. However, the response time was anyway lower for the samples, sensitized in the 0.01 M Ru (OH) Cl3 solution. For these sensors, it was equal to ~30–40 s while the response time for the samples sensitized in the 0.03 M Ru (OH) Cl3 solution was equal to ~2–3 min. A limitation of the sensor is its slow recovery after the gas supply is stopped. The prepared sensors made of nanocomposite MWCNT/SnO_2/Pd and sensitized with ruthenium were maintained in the environment of isobutane gas for 24 h with the aim of improving the sensor characteristics. Despite some reduction in the response, it has led to faster sensor recovery (the recovery time decreased down to 2–3 min). In order to improve characteristics, the second annealing after a sensitization with ruthenium was carried out at higher temperatures (650°C and 850°C). The dependence of the response on the concentration of isobutane is almost linear for the MWCNT/SnO_2/Pd sensors. For them, almost the same times of response and recovery were observed. They are equal ~30–40 s at low concentrations of the gas. Note that parameters of these structures remained stable at a rather long-term testing of sensors. The sensitization of MWCNT/SnO_2 nanocomposite with Ru catalyst leads to sharp rise in response to methanol and ethanol vapor up to 10^3 and higher. At that, the cross-sensitivity to other gases decreases. The response to methanol and ethanol vapors appears at the operating temperature of 200°C and decreases exponentially with temperature rise up to 300°C. Such a fictionalization with Ru leads to appreciable increase in response to i-butane. It is observed beginning from gas concentration 50 ppm. The typical response and recovery times of such i-butane sensors at operating temperature of 200°C are 5–7 s and about one minute, respectively. The increase in operating temperature up to 250°C leads to sharp decrease in both response and recovery times down to 1–2 s and 10 s, respectively. The sensitivity remains practically the same; therefore if priority is given to faster response behavior, slightly elevated 250°C operating temperature can be selected. With the following increase in operating temperature (≥300°C), adsorbed oxygen desorbs increasingly from the surface. As a result, the response to i-butane sharply decreases. The surface-ruthenated nanocomposite containing large amount of SnO_2 (1:50) nanocrystallites show high response both to methanol and ethanol vapors. Simultaneously, relatively high response to i-butane is also observed. Approximately the same sensitivity to alcohols (about 10^3) remains at the 1:8 ratios of the nanocomposite components but the response to i-butane sharply decreases. The re-

sponses to hydrogen and i-butane disappear completely with the following decreasing of SnO_2 part in the nanocomposite (at 1:4 weight ratios of the components).

Thick-film VOCs sensors based on reheated multi-walled carbon nanotubes coated with tin-dioxide nanoparticle nanocomposite structures (MWCNTs/SnO_2) shown that the optimal conditions for applications as acetone, toluene, ethanol and methanol vapors sensors in view of high response and selectivity relative to each other depend on choice of material synthesis method, mass ratio of the nanocomposite components and selected operating temperature. MWCNTs/SnO_2 sensor structures having the mass ratio of the components 1:4 and 1:24 exhibit selective sensitivity to acetone and toluene vapors at 150^{o}C operating temperature, respectively.

With increase in operating temperature, the response to acetone vapor raises up to 360.4 value at достаточно высокой while the selectivity remains sufficiently high. The largest response to acetone vapors (R_a/R_g=555,62) in steady-state regime (formed after the first acetone vapor influence) is fixed for the set of samples with 1:200 mass ratio of the components to 1000 ppm acetone vapors exposure at 250^{o}C operating temperature. Response and recovery times of these sensors are about 22 and 27 s, respectively.

Thin film ethanol sensors made from α-Fe_2O_3 decorated with MWCNTs (25:1 weight ratios) shown good response to ethanol vapors already at work body temperature of 150°. One dimensional (1D) coaxial nanotubes of Fe_2O_3 based on carbon nanotubes (CNT-Fe_2O_3) were synthesized via atomic layer deposition using ferrocene and oxygen as precursors. CNTs were suitable for such system only if they were chemically functionalized. Nitrogen-doped CNTs (N-CNTs) contributed atomic layer deposition-Fe_2O_3, and various 1D heterostructural coaxial nanotubes were obtained with well-controlled growth of Fe_2O_3 on N-CNTs. Such heterostructural coaxial nanotubes of CNT-Fe_2O_3 may find great potential applications in photocatalysis, gas-sensing, and magnetic fields. $Co_{1-x}Ni_xFe_2O_4$/MWCNT nanocomposite (x = 0.2, 0.4, 0.5, 0.6, 0.8) were synthesized via an in situ solvothermal method using ethylene glycol as solvent. Such nanocomposites have a high selectivity for ammonia. A composite film of cobalt oxide nanosheet and carbon nanotube adsorbs or desorbs CO gas. The adsorption of a small quantity of CO leads in a dramatic change of the CNT conductivity. Therefore, CNT are suited to detect species at low concentrations (e.g. low ppb level). Such a micro carbon monoxide sensor integrated with a readout circuit on chip manufactured by the commercial 0.35 μm complementary metal oxide semiconductor process and a post-process. The readout circuit is used to convert the resistance of the sensor into the voltage output. The post-process of the sensor includes etching the sacrificial layers and coating the sensing film. The advantages of the sensor include work at room temperature, short response/recovery times and easy post process. Experimental results show that the sensitivity of the CO sensor is about 0.19 34 mV/ppm, and the response and recovery times are 23 sec and 34 sec at 200 ppm CO, respectively. Nano-composite structures made from cobalt oxide and SWCNTs for a gas sensor application (NO_x and H_2) show a response of ~200% upon exposure to 4% H2 at room temperature. CuO/ MWNT thin film based ethanol-sensors had maximal sensing response at an operating temperature near 400 ˚C.

Gas sensors have fabricated based on non-doped and 1 wt% MWCNT-doped tungsten oxide (WO_3) thin films using the powder mixing and electron beam evaporation technique. Hydrogen sensing properties of the thin films have been investigated at gas concentrations ranging from 100 ppm to 50,000 ppm. The results indicate that the MWCNT-doped WO_3 thin film exhibits high sensitivity and selectivity to hydrogen at reduced operating temperatures.

Room Temperature Sensors

Above reported composite sensors still operate at rather high temperatures. Only several authors detected several gases using metal oxide-CNT sensors operated without pre-heating of work body. As it will shown below, such sensors had much better response and shorter response-recovery time, compared to those of sensors made from metal oxide (for example, SnO_2) or CNT material alone.

A SnO_2/MWCNT composite-based NH_3 sensor working at room temperature was fabricated by standard thin film microelectronic technique using both MWCNTs and nanosized SnO_2. At room temperature, the optimal composite sensor exhibited much higher response and faster response-recovery (less than 5 min) to NH_3 gas of concentrations ranging from 60 to 800 ppm, in comparison with the CNT-based NH_3 sensor. 10 wt% MWCNTs/SnO_2 composite was calcined at 500 ◦C in vacuum of 10^{-2} Torr. As expected, the resistance of the sensor increases upon exposure to electron donating gas NH_3.

An increase in the sensor resistance can be hypothesized that the composite sensing layer behaves as a p-type semiconductor. Probably, the response of the composite sensor should be mainly contributed by the MWCNTs, which have been well known to behave as a p-type semiconductor. Comparing with the CNTs-based NH_3 sensor and the SnO_2-based NH_3 sensor reported previously, as-synthesized composites SnO_2/MWCNTs-based sensors have a higher response to NH_3 gas at room temperature.

Gas sensors made from doped-CNT/SnO_2 composites for NO_2 detection at room temperature were reported. Incorporation of CNTs to a SnO_2 matrix results in a dramatic increase in sensor response at very low operating temperatures and even at room temperature. Probably, the main reason for such response enhancement is the co-existence of two different depletion

layers (and associated potential barriers): one at the surface of the metal oxide grains and the other one at the interface between MWCNT and metal oxide. Nitrogen or boron doped CNTs were added into a SnO_2 matrix, which enhances the nanotube conductivity. Such a hybrid sensor was prepared to detect low ppb concentrations of NO_2 in air and shown at least 10 times higher response towards NO_2 at room temperature in comparison with the pristine SnO_2 and N or B-substituted CNT sensors. Nitrogen doped MWNTs sensors exhibited response and recovery times of the order of a few seconds.

It was also established that sensors based on pure tin oxide nanoparticles and on pure plasma treated CNTs did not show responsiveness to nitrogen dioxide and carbon monoxide. In contrast, sensors made of SnO_2-decorated plasma treated CNTs are gas sensitive soon at room temperature. Response time to 1ppm NO_2 was 4 and 3min when sensors are operated at room temperature and 150 °C, respectively.

Sensors made of the mixture of an intermediate amount of tin dioxide precursor (i.e., 20 ml)with 12mg of oxygen plasma treated MWCNTs were also sensitive to CO. However, CO responsiveness was far lower than the one for NO_2. Response time was 5min for 2ppm of CO. Such sensors showed a decrease in resistance with exposure to CO when operated at room temperature. This experimental result is qualitatively consistent with what has been observed. All these research teams have attributed such behavior to the decrease in the work function of SnO_2 in the presence of CO and a decrease in sensor resistance.

The Co_3O_4–SnO_2 material was used. Its maximum sensor response to CO in the working temperature range from 25 to 100 °C was found at 25°C. Doping 0.1% CNT into Co_3O_4–SnO_2 enhanced the CO response of non-doped Co_3O_4–SnO_2. The sensor response varied under CO concentrations ranging from 20 to 1000 ppm.

Pt-doped TiO_2/MWCNT composites have been synthesized by a sol–gel approach, characterized and tested as sensing layer in resistive devices. Regardless the nominal C/Ti molar ratio, only the anatase phase of titania is formed. It was established that the TiO_2/MWCNT composite samples with nominal C/Ti molar ratio ranging from 3.6 to 17.0 were the best. Hydrogen monitoring takes place only with the Pt/TiO_2/ MWCNT ternary sensor, suggesting a synergic action among metal oxide, noble metal and CNTs. Pt acts as a catalytic additive in the Pt-TiO_2/MWNT-based sensors which were found to be sensitive to hydrogen at concentrations between 0.5 and 3% in air. They can be used as hydrogen leak detection devices

It is possible to make sensors on the base of SWCNTs. SnO_2/arc-discharge SWCNT hybrid material based sensor was also developed for the detection of NH_3 and O_3 at room temperature. Sol gel and dip coating techniques was used for preparation of the hybrid sensor which also had an enhanced sensitivity as compared to pure SnO_2 or pure SWNTs based sensors. The detection limit at room temperature was lower than 20 ppb for NH_3 and O_3, respectively. The fast response (few minutes) and a full recovery at room temperature were detected. The H_2 gas sensor was on the base of nanocomposite Co_3O_4 nanocrystals/ SWCNT which is working up to 4% H_2 at room temperature.

On mechanism of response of functionalized sensors to gases

It is obvious today that the doping of metal oxide with CNTs leads to better sensitivity and lower work body temperature of such a hybrid sensor. Several processes take place in such nanocomposites. The full picture of complicate phenomena is not possible to propose today, but we have to take into account the following reasons:

MWCNTs have a huge specific surface area and a nanoscale structure, which exposes a large number of sites at which the gases can react. Detection of various gases can be realized at low temperatures of pre-heating of work body of sensor. Electric conductivity of CNTs is much higher in comparison with the conductivity of metal oxides that can be used to increase the sensitivity of the micro-gas sensors. The CNTs play mostly a role in reducing the resistance of the sensing materials. The metal oxide nanoparticles mainly control the sensing properties. Since metal oxide film has mainly n-type semiconductor characteristics and MWCNTs have p-type, there are two different depletion regions in these hybrid films. Note that the first depletion region is located at the metal oxide surface and the second one is located in the interface between the metal oxide nanoparticles and the MWCNTs.

Creation of nanochannels and formation of p-n or heterojunctions leads to an enhanced gas sensitivity of such a hybridized gas sensor as the change in barrier height or in the conductivity of the metal oxide sensitive layer may modulate the depletion layer at the p–n junction. Latter may cause the improvement in the performance of the gas sensor at low operating temperature.

The higher is the CNTs content the major conducting carriers are in nanostructure. For example, when the MWCNTs/SnO_2 composites are exposed to NH_3 gas, NH_3 molecules may interact with the MWCNTs by replacing the pre-adsorbed oxygen, resulting in oxidation of NH_3 gas at the surface and removing the oxygen accordingly. Therefore, the potential barrier of the hetero-junction formed by MWCNTs and SnO_2 can be modulated and the conductivity of the composite material during the exposure to NH3 gas can be changed.

Apparently, discussed possible mechanisms require further experimental and theoretical investigations. Beside, the response of the composite thin film gas sensor strongly depends on the preparation process of the sensitive film. For example, if the composite thin film with the MWCNTs content of 15 wt%, the MWCNTs diameter of 60–100 nm, the calcinations

temperature of 530 ◦C under vacuum of 10^{-2} Torr, the film thickness of 400 nm is optimal. This result also implies that these conditions need to be optimized for practical applications of the composites of semiconductor metal oxide/carbon.

Conclusion

1. Use of pristine CNT as sensors does not promising.
2. Functionalization of CNTs can be made with organic materials. Hyper sensibility and selectivity of detection of CO_2, NH_3, O_2, Cl_2, HCl, dimetyldimetylphosphate observed by CNT nanocomposites, covered with polyethylene, polyanylyne and polypyrrol.
3. CNTs, decorated with Pd, Rh, Au and Ni nanoparticles are suggested for detection of H_2S, CH_4, H_2, CO, O_3, C_6H_6, NH_3, NO_2, and C2H5OH up to their ppb level.
4. Special interest is attended to investigation of possibilities of manufacture of CNT functionalized (decorated) with different metal oxide composites. Most of its are carried out by CNT, decorated with SnO_2. Modifications of such nanosensors surface with precious metals led to remarkable improve of the sensitivity and selectivity of sensors.
5. Sensibilisation of CNT- SnO_2 composites in water solutions of Ru (OH) Cl3 leads to high response to hydrogen as well as to synenergistic effect during detection of isobutene and the lowering of temperature of pre-heating of work body of sensors up to 150-200^{0}C. Such sensors are sensitive also to vapors of VOC gases (acetone, toluene, ethanol and methanol) at approving the same temperatures of pre-heating.
6. Thin film (including 1D film) nanosensors of ethanol vapors were manufactured on the base of CNT-Fe_2O_3 solid solutions. Sensors of H_2, NO_x and CO were manufactured from CNTs with cobalt oxide, $Co_{1-x}N_xFe_2O_4$, CuO and WO_3.
7. Substantial interest invokes research and development of nanosensors working without pre-heating of their work body (at room tmperature). 10%- SnO_2 –CNT nanocomposit sensor detected ammonia and NO_2. Doping of CNT with N and B and its synthesis with metal oxide SnO2 allowed dramatically increase the conductivity of the nanosensor and response to CO and NO_2. Nanosensors made from Co_3O_4- SnO_2 and Pt/TiO_2/CNT was sensitive to H_2, NH_3 and O_3 on the 20 ppb level of gas concentration.
8. Nanosensors made from all mentioned composites CNT-metal oxides had lowest response and shorter times.
9. It is clear that the doping of metal oxides with CNTs lead to greater sensitivity to gases, better speed to response of nanosensors and a lowering of temperature of pre-heating of their work body (up to room temperature, when the pre-heating is not necessary). Possible mechanisms of the response of developed sensors to gases are discussed. Doubtless, that different type of conductivity of CNTs and metaloxides, change in the work function (higth of potential barrier), modulation of formed heterujunctions should be take into account at the analysis of complicate processes and phenomena in gas sensitive structures reported above.

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ON SELECTIVITY OF SURFACE-RUTHENATED MWCNT/SnO_2 NANOCOMPOSITE VOCs SENSORS

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1. Introduction

Advancement of the sensing technology is generated by a need of humankind safety and security as well as monitoring of air pollution, because the last one can cause a number of diseases. The main air pollutants are some inorganic gases or various volatile organic compounds (VOCs). Toxic and pollutant VOCs such as acetone, toluene, dimethylformamide, ammonia and butanol are indoors. The main sources the same VOCs outdoor are industrial emissions combustion processes, traffic vehicles and fuel evaporation [1]. Therefore, gas sensing devices installation in such places and development of advanced monitoring systems for their early detection are indispensable. Acetone is widely used in industry and research laboratories for dissolve plastic, purify paraffin, and dehydrate tissues in pharmaceutics. Inhalation of acetone causes headache, fatigue and even narcosis and harmfulness to nerve system. Highly sensitive acetone gas sensors are essential for identification of diabetes and monitoring health conditions and treatment of diabetic patients [2]. Dimethylformamide has been linked to cancer in humans, and it is thought to cause birth defects. Ammonia is highly toxic to aquatic animalseven at dilute concentrations, and for this reason it is classified dangerous for the environment.

Gas sensors based on nanostructured semiconductor metal-oxides materials such as nanoparticles, nanowires, hollow spheres and others, or their nanocomposites with carbon nanotubes (CNTs) [3-6] are considered more promising in gas detection systems and devices. CNTs in themselves possess by a number of useful behaviors such as a wide range of electrical properties, small size, high structural and chemical stability, high strength and so on.

As it was shown in [4], the functionalization of multi-walled carbon nanotube (MWCNT)/SnO_2 thick-film structures by Ru leads to considerable increase in response signal to methanol and ethanol vapors as well as to i-butane gas. However, the selectivity problem of studied sensors relative to other gases, particularly to some harmful and toxic VOCs exposure remained not solved.

In this paper, we report different vapors sensing properties of various ruthenated MWCNT/SnO_2 nanocomposite structures. The choice of corresponding treating conditions and regimes for CNTs functionalization as well as thick films surface modification with Ru catalyst were focused on obtaining the sensitivity to mentioned target gases.

Thick-film sensors are prepared by using 2 methods: hydrothermal synthesis and sol–gel technique. It is shown that the optimal conditions for butanol, dimethylformamide, ammonia, formaldehyde, acetone, toluene, methanol and ethanol vapor sensors in view of high response and selectivity relative to each other depend on choice of material synthesis method, mass ratio of the nanocomposite components and selected operating temperature. Sensors prepared with hydrothermal synthesis demonstrate selective sensitivity to acetone and butanol vapors at 200^{o}C operating temperature. Sensor structures having the mass ratio of the components 1:4, are mainly sensitive toward acetone and butanol vapors in the range of 150-250^{o}C operating temperatures. The samples with 1:200 mass ratios of the nanocomposite components exhibit selective sensitivity to acetone and toluene at 250^{o}C operating temperature [7]. High response to methanol and ethanol vapors is demonstrated with the sensors prepared using sol–gel technique at 200^{o}C operating temperature. The last ones also exhibit high selective sensitivity to butanol at 250^{o}C operating temperature.

2. Experimental

2.1. Preparation of the Materials

MWCNTs/SnO_2nanopowders for thick film preparation were made in the following two ways: using sol–gel preparation technique and hydrothermal synthesis. The sol-gel and hydrothermal synthesis processes as well as material and samples preparations are in detail presented in [4], therefore, there is no necessity to present them here once more. We note only that the final mass ratios of the MWCNT/SnO_2 nanocomposite obtained with a hydrothermal method were, respectively, 1:4 and 1:200 but one with a sol-gel method was 1:50.

2.2. Gas sensing measurements

VOCs vapors sensing properties of the MWCNTs/SnO_2 composite structures were measured by homemade developed computer-controlled static gas sensor test system [4]. The sensors were re-heated at different operating temperatures. When the resistances of sensors were stable, saturated target vapor was injected into a measurement chamber by a microsyringe. The target gases, including the vapors were introduced in the measurement chamber on special hot plate designed for the quickly conversion of the liquid substance to its gas phase (≤12 s). After the sensor resistances reached a new constant val-

ue, the test chamber was opened to recover the sensors in air. The gas response S of the sensors was determined as R_a/R_g where R_a and R_g are the electrical resistances in air and in target VOCs-air mixed gas, respectively.

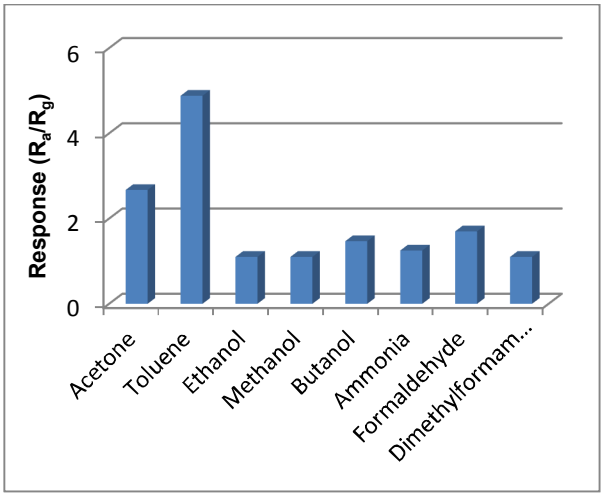

Fig 1. Comparison of the response of samples with 1:50 weight ratios of the nanocomposite components to 1000 ppm different VOC exposure at 150°C operating temperature.

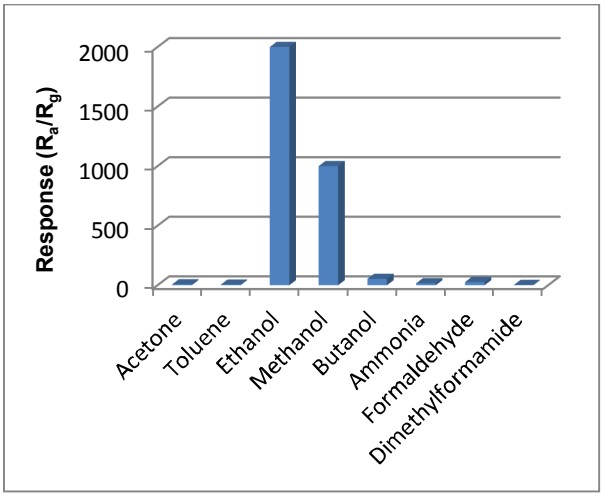

Fig 2. Comparison of the response of samples with 1:50 weight ratios of the nanocomposite components to 1000 ppm different VOC exposure at 200°C operating temperature.

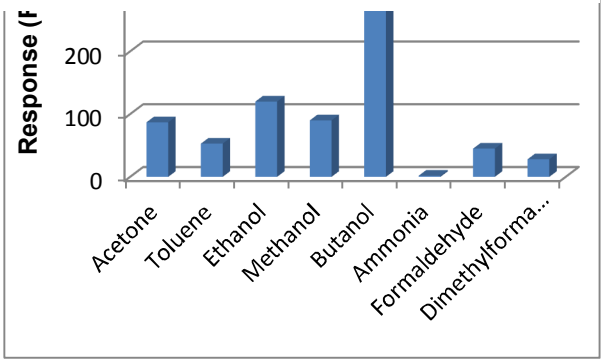

Fig 3. Comparison of the response of samples with 1:50 weight ratios of the nanocomposite components to 1000 ppm different VOC exposure at 250°C operating temperature.

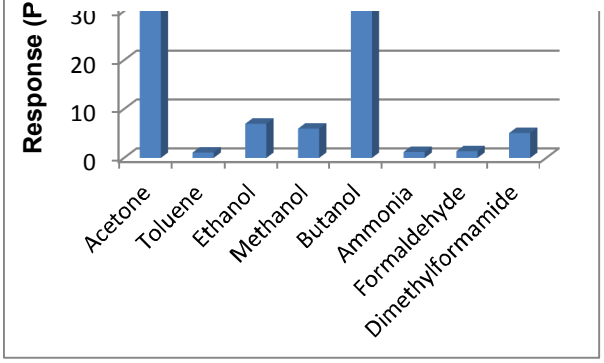

Fig 4. Comparison of the response of samples with 1:50 weight ratios of the nanocomposite components to 1000 ppm different VOC exposure at 300°C operating temperature.

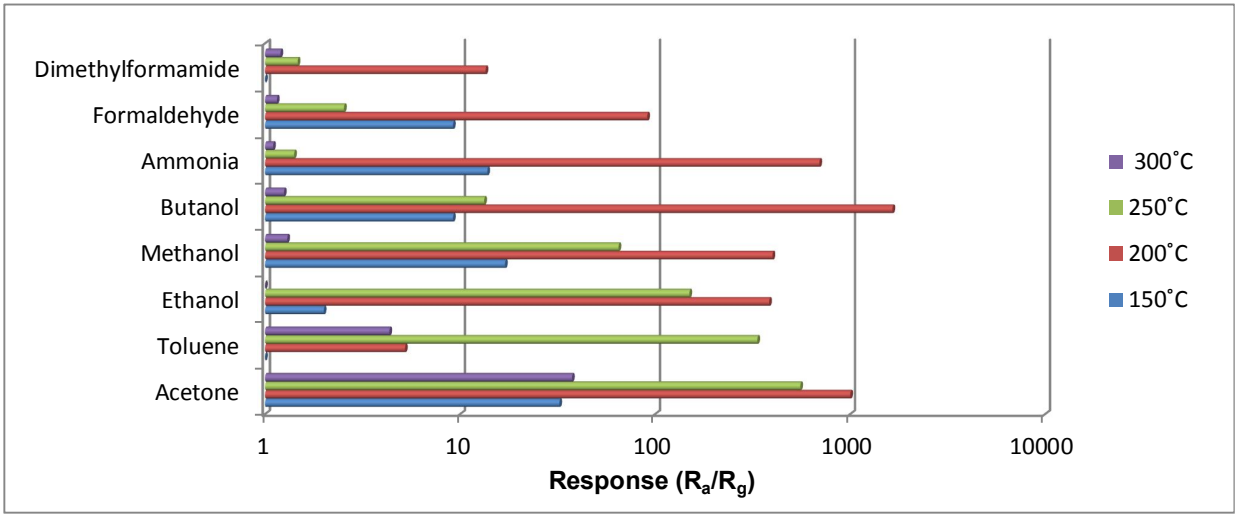

Fig 5. Response of samples with 1:200 weight ratios of the nanocomposite components to 1000 ppm of studied VOCs exposure vs operating temperature.

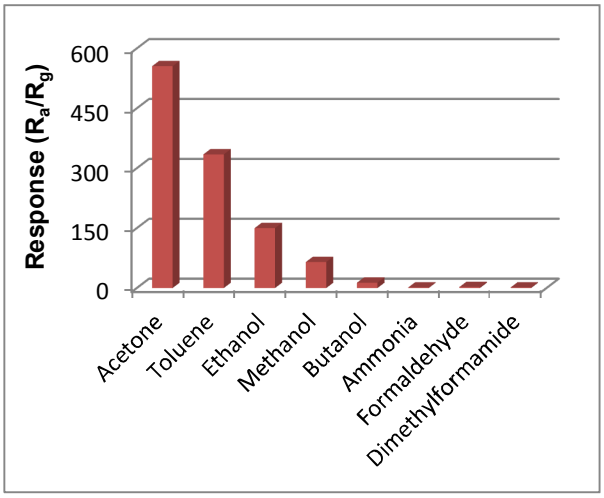

Fig 7. Comparison of the response of samples with 1:200 weight ratios of the nanocomposite components to 1000 ppm different VOC exposure at 250°C operating temperature.

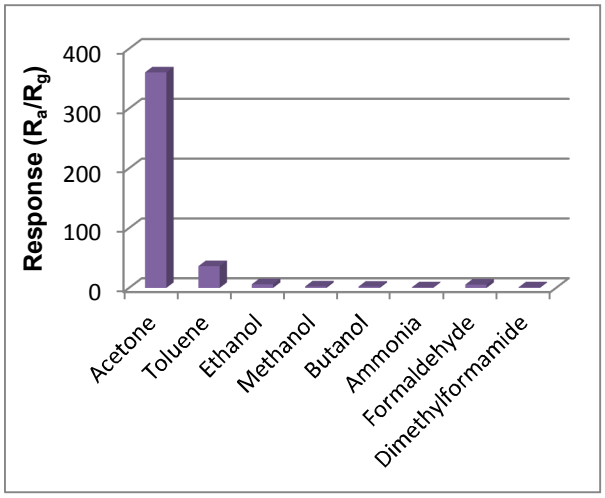

Fig 6. Comparison of the response of samples with 1:4 weight ratios of the nanocomposite components to 1000 ppm different VOC exposure at 250°C operating temperature.

The response and recovery times are determined as the time required for reaching 90% resistance change from the corresponding steady-state value of the signal.

2.3. Gas sensing characteristics

It is interesting to mention that the sensors prepared with sol–gel technique exhibit selective sensitivity to different vapors at different operating temperatures. As it is shown in Fig. 1, these sensors demonstrate not high but selective sensitivity to toluene vapor at 150°Coperating temperature. With the increase of the operating temperature, the response to ethanol and methanol vapors rises up, and the sensors exhibit high selective sensitivity to these vapors at 200°Coperating temperature (Fig. 2). Responses to ethanol, methanol and other vapors are poor compared with response to butanol vapor at 250°Coperating temperature. Hence, at that operating temperature, we have sensor with high selective sensitivity to butanol (Fig. 3). Finally, not so high but selective response of the sensors to acetone and butanol vapors is demonstrated at 300°C operating temperature (Fig. 4). Sensor structures prepared using hydrothermal synthesis and having the mass ratio of the components 1:200 exhibit no selective sensitivity in the range of 150-250°C operating temperatures. By increasing operating temperature from 150°C to 200°C sensitivity increases too, but the sensors continue to demonstrate response to acetone, ethanol and methanol vapors as well as to butanol and ammonia vapors (Fig. 5). High selective response to acetone and toluene vapors is demonstrated at 250°C operating temperature (Fig. 6). The sensors exhibit selective sensitivity to acetone only at 300°C operating temperature. Compared with the last ones, the samples with 1:4 mass ratio of the nanocomposite components exhibit high selective sensitivity to butanol and acetone respectively at 200°C and 250°C operating temperatures (Fig. 7).

3. Conclusion

Conditions are determined at which the studied MWCNTs/SnO_2 nanocomposite gas sensors exhibit the selective reaction to various vapors. Selectivity of the sensors prepared with sol–gel technique to different vapors depends on selected operating temperature. The sensors exhibit selective sensitivity to various vapors at different operating temperatures. Compared with them, samples prepared with hydrothermal synthesis demonstrate different responses depending on mass ratio of the nanocomposite components. Sensor structures with the mass ratio of the components 1:4are more selective and exhibit high sensitivity to butanol and acetone accordingly at 200°C and 250°C operating temperatures. The samples with 1:200 mass ratios of the nanocomposite components start to demonstrate selective response to acetone and toluene at250°C operating temperature but the selective response only to acetone vapors is observed at 300°C operating temperature.

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DETECTION OF GASOLINE VAPOR BY ZnO THIN FILM SENSOR

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1. Introduction

ZnO is a wide band gap (3.37 eV) semiconductor. Due to its high thermal and chemical stability, it is widely used in solar cells, optoelectronic devices, semiconductor resistive gas sensors, etc [1-5].

Zinc oxide as a gas sensing material is used in semiconductor gas sensor made of: resistive thin film with nanosized grains, nanowires, nanofibers, nanotubes and so on. Such sensors exhibit high sensitivity to various gases (H_2, NO, alcohol, gasoline, toluene, dichlorethan vapors, etc) [6-10].

As we know, gasoline is used in various fields. Especially, it is widely used as a fuel. Cars need in the gasoline high response and selectivity sensors. They should fast detect the gasoline leakage. High precision control of the air-fuel ratio in vapor control system of car engine is necessary [11,12]. There are fuel level non-semiconductor sensors produced by Dongguan Manufacturer, etc. They are complicated, it is necessary to develop microelectronic semiconductor sensors.

It is known that the key parameters of resistive thin film gas sensors depend on the thickness of a sensing layer. Especially, the increase in the response of thin film sensor with decreasing of the sensing layer thickness was observed. Besides, there is an opposite dependence (an increase in the response on the thickness) [13-20]. As we shown below, the first dependence is typical for our samples.

Resistive thin film gas sensors with derrerent thicknesses made of the ZnO+1at%La structure with nanosized grains were prepared by us. The thin film sensor with the film thickness of 80 nm has enhanced response and selectivity to gasoline vapor.

2. Experimental

ZnO-based gas sensing films were deposited by magnetron sputtering method from previously prepared ceramic target. Metal oxide starting materials (powders) were weighted in appropriate quantities (ZnO+1at.%La) and mixed for approximately 10 hours. Then, this mixture was subjected to preliminary heat treatment in the 800^0C-1100^0C temperature range. The resulting mixture was pressed (using the 2000 N/cm^2 pressure) in a form of the 50 mm diameter tablet and annealed. Annealing was performed in software-controlled furnace (Nabertherm, HT 04/16) at different temperatures (1000^0C-1400^0C). Then, the sample was subjected to mechanical treatment in order to eliminate surface defects and obtain the smooth, parallel target with the appropriate thickness (<2 mm) and diameter (40 mm). The ZnO+1at.%La gas sensitive thin films with different thichnesses were deposited on alumina substrate by the rf magnetron sputtering method using obtained ZnO+1at.%La ceramic target. The growing film thickness was cntroled by the changeing of the sputtering time when the power of the magnetron generator unit was fixed. The sputtering duration equals to 10, 15, 30, 45 minutes and the power of magnetron generator unit was 60 W. The substrate temperature during sputtering was 200 ^{0}C. Palladium (Pd) catalytic particles (the deposition time was 2 seconds) and interdigited titanium (Ti) contacts (the deposition time was 50 minutes) were deposited by ion beam sputtering method on the surface of the sensing layers. The obtained thin film with sputtering duration of 10 minutes was enough thin (the layer was not continuous) and had an extremely high electrical resistance (10^{12}ohm). The film with sputtering duration of 45 minutes was enough thick (400 nm) and exhibited poor sensitivity to gasoline, toluene and dichlorethan vapors. So, here only the sensing results of the thin films with sputtering duration of 15 and 30 minutes are presented.

3. Results and discussion

The thicknesses of the ZnO+1at.%La films with sputtering duration of 15 and 30 minutes were measured by Ambios XP-1 profilometer, which are 80 and 210 nm, respectively (see Fig. 1). The response (the ratio of the resistance of the sample in air to the resistance in gasoline vapor, R_{air}/R_{gas}) of the semiconductor ZnO+1at.%La sensors to gasoline, toluene and dichlorethan vapors were measured in different temperature range of the work body by gas measurement system [21]. The corresponding responses for the two sensing layers with different thicknesses are presented in Fig. 2. The thinner (80 nm) ZnO+1at.%La based structure exhibits better response to gasoline vapor. The reduction of the sensing layer thickness enhances the sensor response more than four times.

The response of the ZnO+1at.%La film to different concentration of gasoline vapor is shown in Fig. 3. The response of the sensor increases rapidly with increasing in the concentration of gasoline vapor. It is also clear that both the response and recovery times improve with increasing in gasoline vapor concentration.

Fig. 4 shows the resistance change of the ZnO+1at.%La sensor in the presence of 1000 ppm gasoline vapor concentration. It is clear that the response and recovery times are 30 and 130 s, respectively.

The variation of response of the ZnO+1at.%La sensors as a function of workbody temperature is shown in Fig. 5. The sensitivity increase with the workbody temperature increasing was also observed. The plots indicate that there is an approximately linear relation between the response of the La-doped ZnO sensors and the work body temperature for both 80 and 210 nm thicknesses of sensing layers.

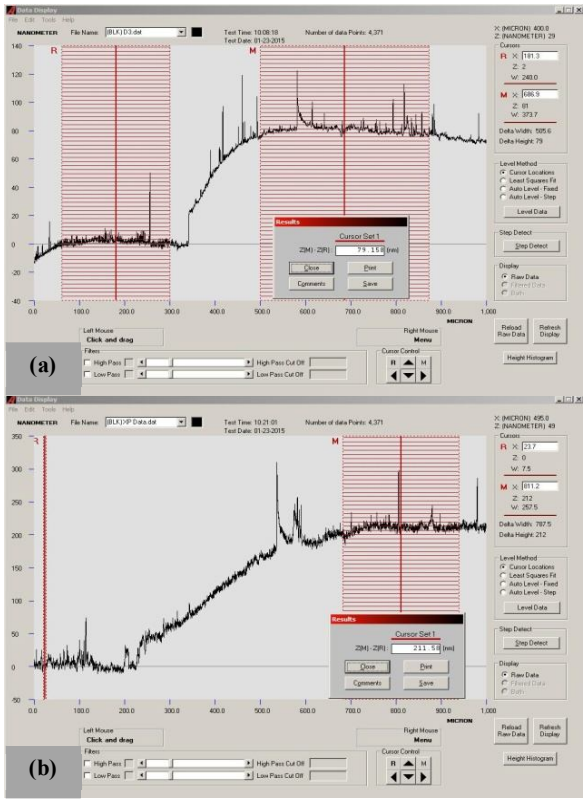

Fig.1.The ZnO+1at.%La films thichnesses measurament resultes with sputtering duration of 15 (a) and 30 minutes (b).

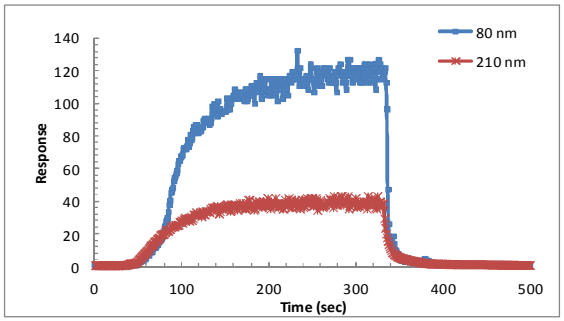

Fig.2.The response curves of the ZnO+1at.%La sensors (with thicknesses of 80 and 210 nm) to 2000 ppm gasoline vapor concentration (the work body temperature was 350 ^{0}C).

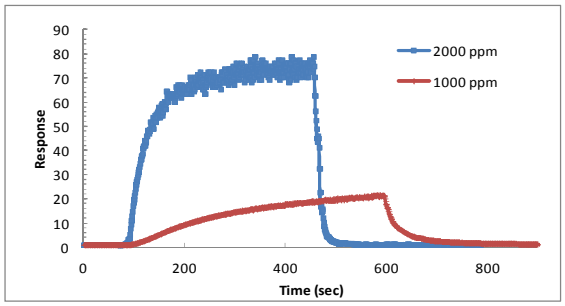

Fig. 3.The real-time response curves of the ZnO+1at.%La sensor (withthickness of 80nm) to various concentration of gasoline vapor (the workbody temperature was 300 ^{0}C).

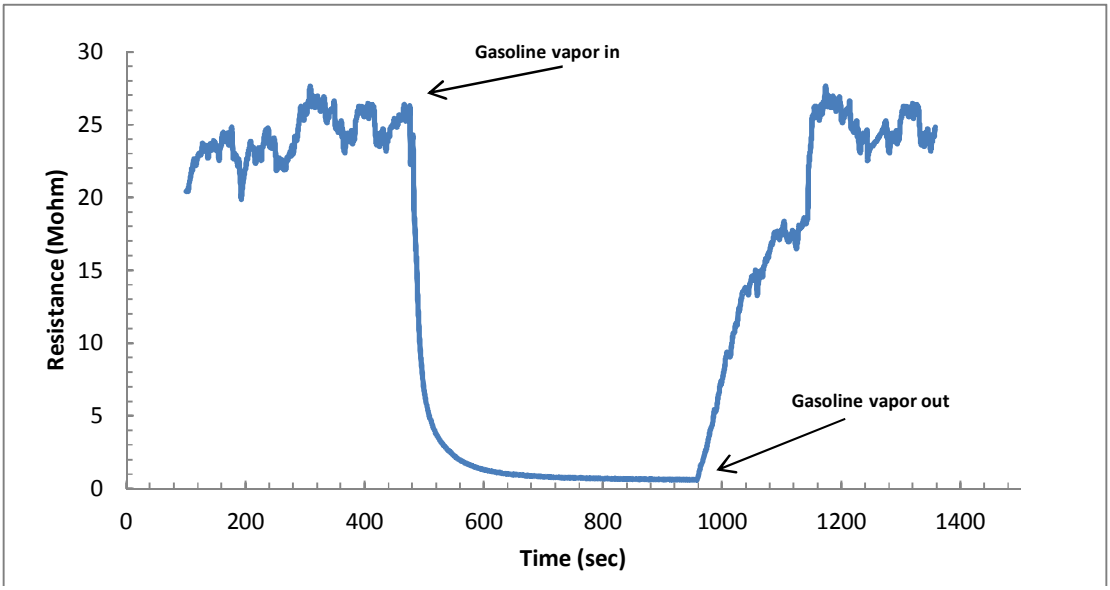

Fig. 4.The variation of the resistance of the ZnO+1at.%La sensor (withthickness of 80nm) for 1000 ppm gasoline vapor concentration (the workbody temperature was 350 ^{0}C).

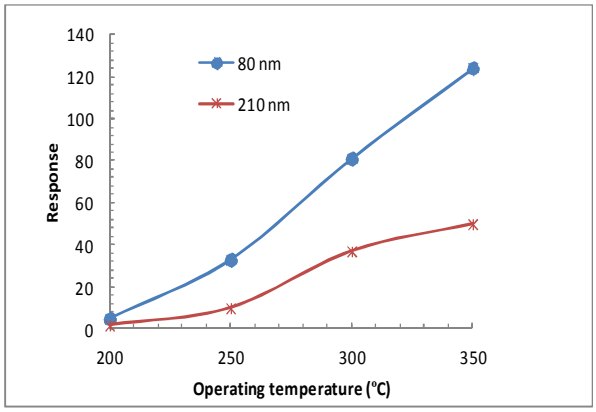

Fig. 5.The relationship of the ZnO+1at.%La sensors response and operating temperature for 2000 ppm gasoline vapor concentration.

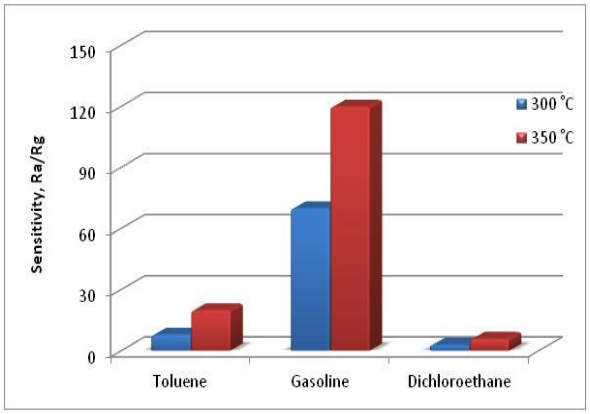

Fig.6. The sensitivity and selectivity of theZnO+1at.%La sensor to different gases (2000 ppm concentration) at different work body temperatures.

It is know that the poor selectivity is serious problem for the practical useable gas sensors. The selectivity of the La-doped ZnO sensor (with thickness of 80 nm) toward other gases such as toluene and dichlorethane vapors was also investigated. The sensor exhibits high selectivity toward gasoline vapor at different work body temperatures (see Fig.6).

4. Conclusion

The La-doped ZnO sensitive thin films with different thichnesses were fabricated by the rf magnetron sputtering technology. The response and selectivity behaviors of the ZnO+1at.%La sensors were investigated. The sensing results indicated that the response of the gas sensor with 80 nm thickness is higher than that of 210 nm. The ZnO based sensor (with 80 nm thickness) exhibits high sensitivity (120) and selectivity to small concentration of gasoline vapor. The response and recovery properties of the sensor are also appreciable. Therefore, it can successfully serves as gasoline vapor detector.

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AUTOMATIC SYSTEM FOR SEMICONDUCTOR GAS SENSOR FLICKER-NOISE MEASUREMENT

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1. Introduction

Flicker-noise (F-N) presents a current or voltage fluctuations, which spectral density changes along with frequency as $1/f^{\nu}$, where value of coefficient ν ranges between from 0.6 and 3 (determined by experiment) [1]. F-N – is a widespread and universal phenomenon in electronic devices. Despite the fact that F-N investigation conducted for a considerable length of time, a general theory of this noise has not been developed yet.

F-N investigations have theoretical as well as a great practical importance, since F-N essentially deteriorates characteristics of electronic constructions and devices, running in low-frequency noise region. F-N can also serve as diagnostic means for semiconductor devices. Successful application of indestructible control method to semiconductor devices by low-frequency noise parameters can be performed with very highquality metrological equipment.

Semiconductorgas sensor (SDS) detection efficiency can be improved bylow-frequency fluctuation-enhanced sensing [2]. Therefore, an example of gas sensor F-N measurement automatic system constructed using LabVIEW graphical program environment is presented in this study.

2. Measurement Method

Noise$u_1(t)$ has extremely small amplitude and therefore requires highamplification.Measurement method idea is in the following – sought-for noise signal $u_1(t)$from investigating gas sensors act on two identical low-noise amplifiers.Considerable own amplifier noise $S(t)$ is incidentally added to amplified noise$U_1(t)$.Therefore chosen measurement method must maximally reduce the effect of amplified noises on measurement result.

One of the noise measurement methods is the following. On Wiring Terminal Board the inputs and outputs of two independent and identical amplifying channels should be connected. This singularly increase the same thing sought for noise signal $U_1(t)$. Since amplifiers' noises are statistically independent, then at corresponding averaging we can exclude amplifiers noise from measurement result. Measurement circuit allows similar averaging based on cross correlation data processing with bi-channel correlative amplifier.

Suppose, there is a sum $U_1 + S_1$on output of first channel with amplification coefficient K, where $U_1(t) = K \cdot u_1(t)$ is the amplified signal; $S_1(t)$ is the own noise of the first amplifying channel. Similarly, on the second channel output – correspondently $U_1 + S_2$. Mutual correlation function $R_{12}(\tau)$is calculated as an average value of amplifier output signal product:

$$R_{12}(\tau) = \overline{\big(\mathrm{U_1(t) + S_1\,(t)}\big)\big(\mathrm{U_1(t-\tau) + S_2(t-\tau)}\big)}. \tag{1}$$

By multiplying signals under the average symbol we will receive:

$$\begin{aligned} R_{12}(\tau) &= \overline{\mathrm{U_1(t)U_1(t-\tau) + U_1(t)S_2(t-\tau) + U_1(t-\tau)\,S_1(t) + S_1(t)S_2(t-\tau)}} = \\ &= \overline{\mathrm{U_1(t)U_1(t-\tau)}} + \overline{\mathrm{U_1(t)S_2(t-\tau)}} + \overline{\mathrm{U_1(t-\tau)\,S_1(t)}} + \overline{\mathrm{S_1(t)S_2(t-\tau)}} = \\ &= \overline{\mathrm{U_1(t)U_1(t-\tau)}} = \mathrm{R_{11}(\tau)}, \end{aligned} \tag{2}$$

where $U_1(t)$ is the amplifiers output signals; $S_1(t)$and $S_2(t)$is the noise of the first and second amplifiers; $R_{11}(\tau)$ is the autocorrelation function of $U_1(t)$signal.

In expression (2) all average values of cross products is equal to zero, since factories are statistically independent. Thus, this measurement method circuits make it possible to distinguish autocorrelation function of desired noise $\overline{\mathrm{U_1(t)U_1(t-\tau)}} = \mathrm{R_{11}(\tau)}$ on correlation output.

Energetic spectrum $\mathrm{S_{11}(f) = S(f)}$ is determined from one of two equations of Wiener – Khinchin law [1]:

$$S_{11}(t) = 2\int_{-\infty}^{+\infty} R_{11}(\tau)\cdot e^{-i2\pi f\tau} d\tau = F\{R_{11}(\tau)\}\,. \tag{3}$$

Thus, the correlation function $\mathrm{R_{11}}$ subjected to Fast Fourier transformation (FFT) according to expression (3), we may receive spectral density $S_{11}(f)$ of the studied noise.

3. Experimental installation and program software

In the virtual instrument (VI) functional diagram of F-N spectrum measurement system according to method discussed above, current noise signal fromthe investigating SGS $\mathrm{u_l(t)}$ acts on be-channel low noise amplifier, which is necessary for signal amplification up to input operating range level of analogue-to-digital convertor (Fig. 1).

Correlation amplifiers made and used by us have following parameters: coefficient of amplification is the $K = 10^4$; amplifier bandwidth is the $0 \div 2\ kHz$; input impedance is the 50 MΩ. Amplifiers output signals act on National Instrument Data

Acquisition USB device. Functions of signal processing in LabVIEW program intended for digital processing and analysis of determinate and stochastic signals filtration. *Generation functions* allow signal generation with given parameters.

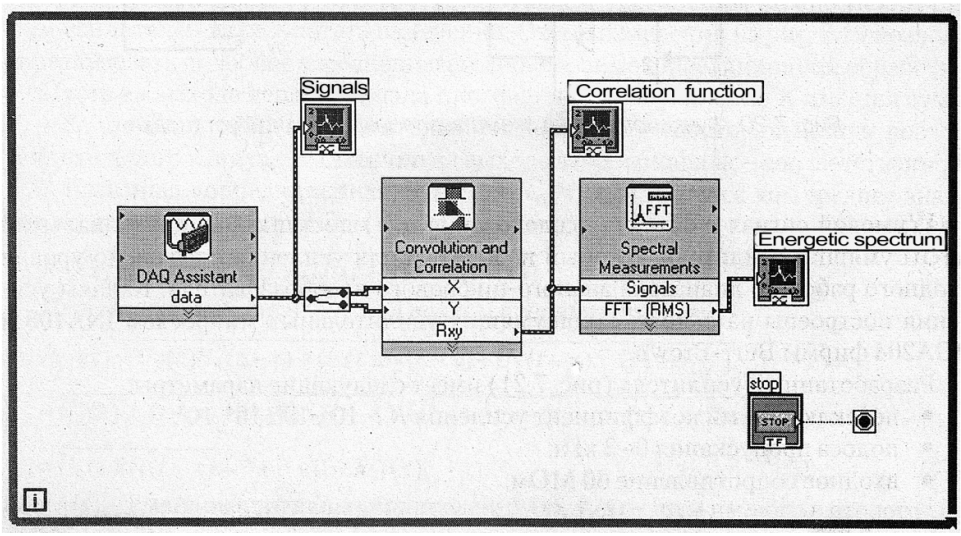

Fig. 1. Flicker-noise measurement VI Block Diagram of LabVIEW program.

Numbering signals processed in LabVIEW program software. Corresponding program for spectral density $S(f)$measurement include three basic procedures: data input to computerize information from NI DAQ USB device; calculation of crosscorrelation function $R_{12}(\tau)$ and calculation of energetic spectrum $S(f)$ [3,4].

Pattern of input-output arrangement configuration and signals input are carried out by built-in LabVIEW drivers. For this purpose an express-device *DAQ Assistant*is used. It opens adjusting window of input-output devices (Fig. 2). In this window we can assign the quantity of polling channels and pattern of their connection (differential or unipolar) the type of measuring signal (voltage, current, frequency, temperature, etc.) the range of input signal the frequency of discretization and regime of signal input in the computer. The latter input regime in computer can be programmedin form of one counting out make an inquiry at or over definite time interval, too as well in massive form consistedof N counting out (Fig. 2).

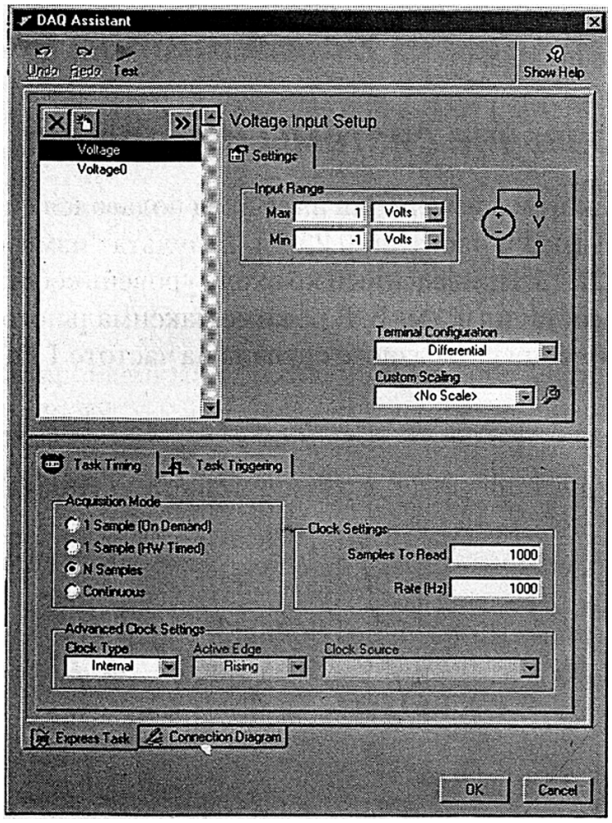

Fig. 2. Adjusting of input-output arrangement by *DAQ Assistant*.

Express-device *Convolution and Correlation* in LabVIEW supplement *Analysis* is used for calculation of cross-correlation $R_{11}(\tau)$ function (in our case the noise measurement of SGS cross correlation function). For this in initialized windows chose calculation of crosscorrelation function *Cross Correlation*. Calculation of energetic spectrum is realized by express-device *Spectral Measurement* - FFT. Calculation of amplitude spectrum *Magnitude*is chose in a respective window (Fig. 3).

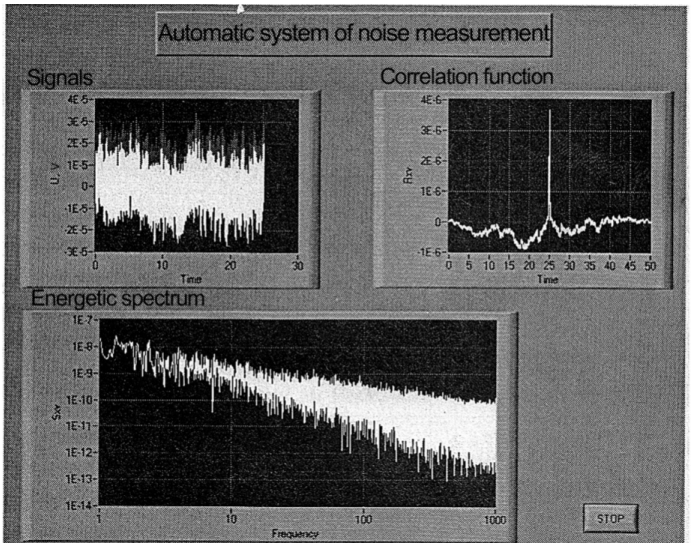

Fig 3. VI Face Panel of SGS noise measurement automatic system.

A sinusoidal signal is provided (amplitude – 1μV; frequency – 0,25Hz) on input this to calibrate and test the installation's structural diagram for investigation of low-frequency noise power spectral density. The result of this measured signal represented on (Fig. 4). Brought to input own noise level of amplifier's channel was 0.1÷ 0.2 μV.

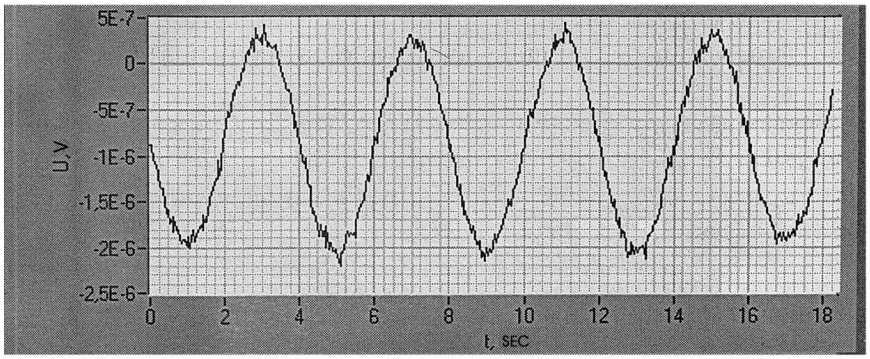

Fig. 4. Testing signal on the output of the noise measuring system (Face Panel).

4. Conclusions

Thus, we presented operationof SGS F-N measurement system constructed by us with the employment of measuring channels in LabVIEW VI graphical environment. Signal analysis in this environment is performed by correlation and spectral analysis which has an essential role in design, planning and experimental investigations of noisy systems. A Face Panel is created for the control and the indication of above-mentioned VI. Input-output adjusting VI is usedby *DAQ Assistant* windows. Calibration and testing of noise measuring channelis carried out by low frequency sinusoidal signal. It is indicated that VI has high noise stability.

Using together the Wiener-Ckinchin law and LabVIEW graphical environment program may provide decreasing the influence of measuring equipment's own noises on measurement results of noise power spectral density investigation.

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NANOSCIENCE & LOW-DIMENSIONAL SYSTEMS

FARADAY ROTATION IN THIN METAMATERIAL FILMS

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1. Introduction

Metamaterials (also called left handed materials (LHM)) are a new type of artificial materials, characterized by having both permittivity $\epsilon$and permeability μ negative [1, 2]. Despite the fact that$\epsilon < 0$ and $\mu < 0$,a metamaterial's refractive index $n =$ dex $n = \sqrt{\epsilon\mu} < 0$ due to the imaginary part of n being positive for [3]. These complex components that cause the negative refractive index make these materials good candidates to form images. For instance, LHM can be used to resolve images beyond the diffraction limit [4, 5], act as an electromagnetic cloak [6, 7], enhance the quantum interference [8] or yield to slow light propagation [9]. The presence of negative indices of refraction in one-dimensional (1D) disordered metamaterials strongly suppresses Anderson localization, due to the lack of phase accumulation during wave propagation, and thus weakening the interference effects necessary for localization [10]. As a consequence, an unusual behavior of the localization length ξ at long-wavelengths λ has been observed [10-12] which is unlike the well-known quadratic asymptotic behavior$\xi \sim \lambda^2$ for standard isotropic layers (see, e.g. [13]).

The metamaterial configurations affect the magneto-optical transport properties of the electromagnetic waves as well. Particularly, the plane of the linearly polarized transmitted light in the external magnetic field $\vec{B}$ rotates clockwise (assuming that wavevector $\vec{k}$and are$\vec{B}$parallel).This is in contrast to behavior of an electromagnetic wave in a right handed medium (RHM), where the plane of polarization rotates counterclockwise, whereϵ, μ, and the Verdet constant of the material are positive.

In the present paper, we theoretically consider the Faraday rotation of light passing through a RHM/LHM film with thickness L, taking into account the multiple reflectionsat the boundaries. It will be shown that the real part of the complex angle of Faraday rotation is an odd function with respect to the refractive index n, while the imaginary part of the angle is an even function of n. We have obtained the rotation angle of backscattered light from RHM/LHM in an ultra-thin film. In LHM thin films, under some circumstances, a large resonant enhancement of the reflectedFaraday rotation angle can be obtained.

Let us first consider a slab confined to the segment $0 \le x \le L$ and characterized by permittivity $\epsilon = n/z$and permeability $\mu = nz$, where$z = \sqrt{\mu/\epsilon}$and is the surface impedance and is a positive quantity for both, right and left handed materials. Both $n$and z, and therefore ϵ andμ, are frequency dependent complex functions that satisfy certain requirements based on causality. It can be shown that for passive materials, $Re(z)$ and $Im(n)$ must be greater than zero.

The two semi-infinite media outside the slab are the same and are characterized by the dielectric constant ϵ_1. A linearly polarized electromagnetic plane wave enters the slab from the left at normal incidence. We take the direction of propagation as the x axis, and that of the electric filed $\vec{E}$ in the incident wave as the z axis. A weak magnetic field$\vec{B}$ is applied in the x direction and confined to the slab.

The generalized principle of symmetry of kinetic coefficients implies that$\epsilon_{ij}(\vec{B}) = \epsilon_{ji}(-\vec{B})$. The condition that absorption is absent requires that the tensor be Hermitian $\epsilon_{ij} = \epsilon^*{}_{ij}$. Then the dielectric tensor of the slab is given by [14].

$$\epsilon_{ij} = \begin{pmatrix} \epsilon & +ig \\ -ig & \epsilon \end{pmatrix},$$

where g describes the magneto-optical properties of the medium.In certain materials (e.g. dielectric) the g is proportional to the external magnetic field B.

The linearly polarized incident electromagnetic wave can be presented as the sum of circularly polarized waves with opposite directions of rotation, which propagate through the slab with different wave vector $k_\pm = \omega n_\pm / c$. In a small magnetic field the effective incident indices of refraction and impedance for the two circular polarizations in the first order of B can be presented in the form

$$n_\pm = \sqrt{\epsilon_\pm \mu} \approx n \pm \frac{1}{2}\frac{gn}{|\epsilon|},$$

$$z_\pm = \sqrt{\mu/\epsilon_\pm} \approx z \mp \frac{1}{2}\frac{gz}{|\epsilon|},$$

where$n$ (the refractive index of a homogeneous material) and z (the impedance of a homogeneous material) are calculated when an external magnetic field $\vec{B}$ is zero.Note that by replacing n with $-n$ we can use the above expressions for LHM.

2. Real Part of Faraday Rotation in RHM/LHM: Transmission

To proceed further, we need to know the explicit analytical expression $t_{\pm}$ for waves incident normally to the face of a 1D slab of continuous material with length L, n and z. To calculate $t_{\pm}$, we follow[14] closelyand solve for the 1D Maxwell equation with the appropriate boundary conditions at $x = 0$ and$x = L$. Doing so, we arrive at the following expressions for $t_{\pm}$:

$$t_{\pm} = T_{\pm}^{1/2} e^{-i\omega L n_{\pm}/c} e^{i\psi_{\pm}}, \tag{1}$$

where the coefficient of transmission $T_{\pm}$ and the phase $\tan\psi_{\pm}$ are given by the following expressions, respectively

$$T_{\pm}^{\frac{1}{2}} = \left[1 + \frac{1}{4}\left(z_{\pm} - \frac{1}{z_{\pm}}\right)^2 sin^2(\omega L n_{\pm} / c)\right]^{-1/2}, \tag{2}$$

$$\tan\psi_{\pm} = \frac{1}{2}\left(z_{\pm} - \frac{1}{z_{\pm}}\right)\tan(\omega L n_{\pm}/c). \tag{3}$$

The imaginary and real parts of the complex FR angle can be defined as (see, e.g., [14])

$$\theta^T = -\frac{i}{2}\ln\frac{t_+}{t_-} = \frac{\psi_+ - \psi_-}{2} - \frac{i}{2}\ln\frac{T_+^{1/2}}{T_-^{1/2}} \tag{4}$$

As is shown in Eq (4), if$T_+ = T_-$, then θ^T would be real; this signifies that the wave remains linearly polarized with vector $\vec{E}$ rotated through the angle θ^T. If $T_+ \neq T_-$, then the light has real Faraday rotation and gains an elliptical polarization. The ratio of ellipse semi-axes is determined by relation $(b < a)$

$$\frac{b}{a} = |\tanh Im\,\theta^T| = \frac{\left|T_+^{\frac{1}{2}} - T_-^{\frac{1}{2}}\right|}{\left|T_+^{\frac{1}{2}} + T_-^{\frac{1}{2}}\right|}$$

and angle χ between the large axis of the ellipse and the axis $0y$ is

$$\chi = Re(\theta^T) = \frac{\psi_+ - \psi_-}{2}$$

One can simplify and proceed with the analysis of $Re(\theta^T)$ and $Im(\theta^T)$ by expanding $\psi_{\pm}$ around the n and z of the slab in the absence of the magnetic filed $\vec{B}$. Then the Taylor series of $\psi_{\pm}$ in the neighborhood of n, z become:

$$\psi_{\pm} = \psi(n,z) \pm \frac{1}{2}\frac{gn}{|\epsilon|}\frac{\partial}{\partial n} \mp \frac{1}{2}\frac{gz}{|\epsilon|}\frac{\partial}{\partial z}.$$

Hence,

$$Re(\theta^T) = \frac{\psi_+ - \psi_-}{2} = \frac{1}{2}\frac{gn}{|\epsilon|}\frac{\partial\psi}{\partial n} - \frac{1}{2}\frac{gz}{|\epsilon|}\frac{\partial\psi}{\partial z} = \frac{1}{2}\frac{g}{|\epsilon|}\left(n\frac{\partial\psi}{\partial n} - z\frac{\partial\psi}{\partial z}\right). \tag{5}$$

Evaluating the derivatives $\frac{\partial\psi}{\partial n}$ and $\frac{\partial\psi}{\partial z}$ at $\vec{B} = 0$ magnetic field from Eq. (3) and substituting these expressions into Eq. (5), we get,

$$Re(\theta^T) = \frac{g}{4|\epsilon|}\frac{(\omega Ln/c)\left(z + \frac{1}{z}\right) - \left(z - \frac{1}{z}\right)\sin(\omega Ln/c)\cos(\omega Ln/c)}{1 + \frac{1}{4}\left(z - \frac{1}{z}\right)\sin^2(\omega Ln/c)}. \tag{6}$$

This is a general expression and valid for a continuous material with the arbitrary parameters L, n and z. As expected, $Re(\theta^T)$is odd in$n$, i.e., in LHM it will change the sign. Below we analyze some of its limits: First, when$L$tends to zero, the above equation reduces to

$$\theta^T \approx \frac{g\omega L}{2c}\frac{\epsilon}{|\epsilon|}, \tag{7}$$

which coincides with the result of[16,17].Second, if$z = 1$, i.e. light propagates in a homogenous medium, it can be shown that

$$\theta_1^T \approx \frac{g\omega L}{2c|\epsilon|}\sqrt{\mu\epsilon}, \tag{8}$$

which coincides with the result of Refs.[14, 16] for the case$\mu = 1$.

3. Imaginary part of FR in RHM/LHM: Transmission

Using the procedure outlined above, we can similarly derive the expression for the of Faraday rotation.

$$Im(\theta^T) = \frac{1}{2}\ln\frac{T_+^{1/2}}{T_-^{1/2}}.$$

The only difference now is that we need to expand $T_\pm^{1/2}$ around the n and z of the slab in the absence of the magnetic field $\vec{B}$ and use the Taylor series for $\ln(1+x)$ around 0. Finally, we find

$$Im(\theta^T) = \frac{g}{8|\epsilon|}\frac{(z^2-1)\sin(\omega nL/c)\left[(1+\frac{1}{z^2})\sin(\omega nL/c) - (\omega nL/c)\,(1-\frac{1}{z^2})\cos(\omega nL/c)\right]}{1+\frac{1}{4}(z-\frac{1}{z})^2\sin^2(\omega nL/c)}. \quad (9)$$

This is again a general expression and valid for any arbitrary parameters of L, n and z. As expected, $Im(\theta^T)$is evenin$n$, and $\theta_2^T \to 0$ when L tends to 0.

4. Real and Imaginary parts of FR in RHM/LHM: Reflection

Based on the general expressions of the scattering matrix elements in terms of the transmission and reflection probabilities one can show that for a spatially symmetric barrier the total phase accumulated in a transmission event $\psi^T$is equal to a phase ψ^R in a reflection event. Hence, $Re(\theta^R) = Re(\theta^T)$and $Re(\theta^R)$ will be described by Eq. (6). As for the imaginary part of FR reflection angle we find

$$Im(\theta^R) = \frac{1}{2}\ln\frac{R_+^{1/2}}{R_-^{1/2}} \equiv Im(\theta^T) + \frac{g}{2|\epsilon|}\left(\frac{(\omega Ln/c)\cos(\omega Ln/c)}{\sin(\omega Ln/c)} - \frac{z^2+1}{z^2-1}\right), \quad (10)$$

where the$Im(\theta^T)$is defined in Eq.(9). In the limit of ultra-thin film approximation, when L tends to zero, the above expression reduces

$$\mathrm{Im}\theta^R \approx \frac{\epsilon}{|\epsilon|}\frac{g}{\epsilon-\mu}, \quad (11)$$

As seen from the above expression, $Im(\theta^T)$ is proportional to the extremely small parameter g and in RHM, where$\mu \ll \epsilon$, it is too difficult to measure θ^R as it tends towards 0. However, the situation is very different for LHM, where μ and ϵ can be of the same order of magnitude in certain frequency ranges. For these frequencies it can be been verified experimentally a narrow resonantly enhanced reflection of large angles will be seen.

5. Conclusion

We have considered the Faraday rotation of light passingthrough a right-handed and left handed film with thickness L, taking into account the multiple reflections at the boundaries. In the limit of ultra-thin film large angles of reflection of the imaginary part of Faraday rotation have been theoreticallyshown to occur in LHM (see Equation (11)). These narrow resonantly large angles appear at specific frequency ranges, when $\mu \approx \epsilon$, allowing for easier use and access for experimental work of metamaterials.

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SCREENED COULOMB PROPERTIES OF SEMICONDUCTOR QUANTUM WIRE WITH DIELECTRIC CONFINEMENT EFFECT

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1. Introduction

In recent years, the electron gas (EG) properties of the quasi-one-dimensional (Q1D) semiconductor nanostructures have been the subject of considerable research effort. In the 3D system, Coulomb screened potential decays exponentially in real space and effectively becomes a short-range potential. In the pure 2D nanostructures, a real space statically screened potential at the long-wavelength limit possess the 2D Coulomb-law spatial dependence for the intermediate distances and power-law asymptote tail at the large distances. Therefore, the effectiveness of Coulomb screening in lower dimensions is reduced and it is obviously to assume that the same tendency should go on stronger in the quantum wires (QWr). A realistic semiconductor QWr either can be freestanding or surrounded by the barrier environment. For the Coulomb center-explored semiconductor QWr structures use of the low dielectric constant barrier environment (lower than the semiconductor dielectric constant) is favorable due to the Coulomb interaction enhancement in the QWr (dielectric confinement effect (DC effect)).

In present paper, we explore a problem of point charges pair (excitons and impurities) statically screened properties of the semiconductor QWr in presence of the DC effect.

2. Dielectric confinement affected Q1D screening potential and screening length

Let consider infinitely long semiconductor cylindrical QWr of radius R filled by semiconductor material with the dielectric constant ε_w and embedded in the dielectric barrier environment with the dielectric constant ε_b. A QWr contains a Q1D EG where the electrons there are confined to move in a QWr and are free to move along the axis of the wire by mean linear density n_L. Moreover, a strong confinement condition is accepted in discussing case, assuming that the quantum wire radius R is small compared with the Bohr radius a_0 in the semiconductor bulk samples ($a_0 >> R$). For that case the large asymptotic distances between the interacting particles along the wire axis $|z| >> R$ are essential [1, 2]. As revealed in [3], for the moderate distances εr $(R/z)^2 \ln(|z|/R) \sim 1$ the screened interaction potential of charged particles $-e$ and e takes the Q1D form

$$V(z) = -\frac{e^2}{\varepsilon_w R}\frac{1}{q_L R}e^{-q_L|z|}, \tag{2.1}$$

where $q_L = (q_S^2 + q_d^2)^{1/2}$, $q_S = [(4\pi e^2/\varepsilon_w)(\partial n_V/\partial \mu_0)]^{1/2}$, $q_d = (1/R)\sqrt{2/\varepsilon_r \ln \varepsilon_r}$ and $\varepsilon_r = \varepsilon_w/\varepsilon_b >> 1$.

The foregoing expressions are obtained in the Thomas-Fermi approximation (TFA) that the externally applied charge $-e$ produces only a linear response in Q1D EG when the energy of an electrostatic perturbation is small as compared with the electron Fermi energy ($\mu_0 >> V(\rho, z)$). Then we may expand the density variation $\Delta n_V(\rho, z)$ and obtain in the leading order as $\Delta n_V(\rho, z) = (\partial n_V/\partial \mu_0) V(\rho, z)$. Here qL can be considered the DC effect influenced effective linear screening parameter with the strong dielectric contrast in the heteroboundaries. The screened interaction potential (2.1) is exponentially weak enough outside the spatial region with the linear size $z_L = q_L^{-1}$ along the wire axis and is enhanced on account of small parameter $q_L R$. As it follows, z_L both can be indicate such as the effective Q1D screening length (SL) in DC effect influenced QWr and can be related to the distances over which significant charge separation can occur. At the same time, the screening parameter q_S will be calculated by using corresponding expression of Ref. 4 [Exp. (3.10)], which after simple calculations is given by

$$q_S^{-2} = R^2\left[\frac{\pi^2}{32 r_S} + \frac{K_1}{16}\sqrt{\pi x} + \frac{r_S x}{4} + \frac{K_2}{K_3}\frac{x}{4}\left[\frac{1}{r_S} + \frac{4}{K_3}\sqrt{\frac{x}{\pi}}\right]^{-1}\right], \tag{2.2}$$

where $K_1 \approx 14.91$, $K_2 \approx -15.61$, $K_3 \approx -0.38$, $x = k_B T/R_0$, $k_B T$ is the thermal energy and $R_0 = \hbar^2/2m_w a_0^2$ is the bulk semiconductor effective Rydberg energy, $r_S = (2 a_0 n_L)^{1/2}$ is the interparticle 1D spacing of the free carriers in the units of Bohr radius.

3. Numerical calculation

In order to display numerically the screened Coulomb properties we refer to the model with the PbSe based QWr embedded in the barrier environment. For that case, the following material parameters are adopted [5]: $m_w \approx 0.036\, m_0$, where m_0 is the free electron mass, $\varepsilon_w \approx 23$, $a_0 \approx$ 34 nm, R = 3 nm, the effective bulk Rydberg energy R_0 = 0.9 meV, ε_{b1} = 2 and ε_{b2} = 1 (vacuum). We carried out the numerical analysis of q_S^{-2} in two cases of linear density n_{L1} =1.1x10^{-6} cm^{-1} and n_{L2} =2.2x10^{-6} cm^{-1} for that dielectric constants ratio model values ε_{r1} = 23 and ε_{r2} = 11.5 are used, respectively. To provide the deeper insight into how the SL varies for T and n_L, in Fig. 2 we plot the graphical calculations of SL as a function of the thermal energy k_BT (scaled by the effective Rydberg R_0) for the foregoing effective electron plasma density parameter r_S fixed values.

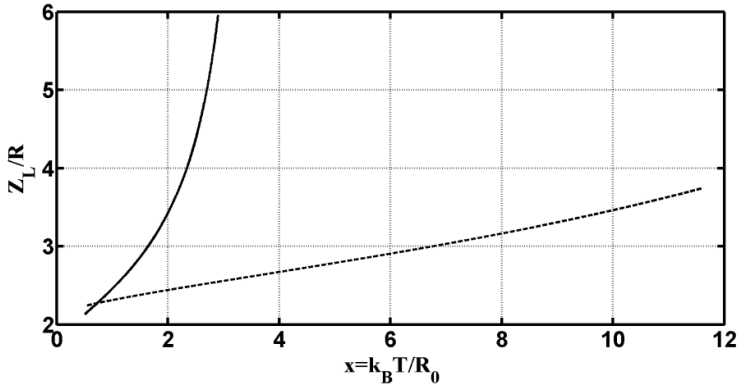

Fig. 2. The SL $z_L = q_L^{-1}$ (scaled by the QWR radius R=3 nm) as a function of the thermal energy k_BT (scaled by the effective Rydberg R_0=0.9eV) for the electron plasma density parameter values r_S = 0.0988 (solid line) and r_S = 0.0494 (dotted line), respectively.

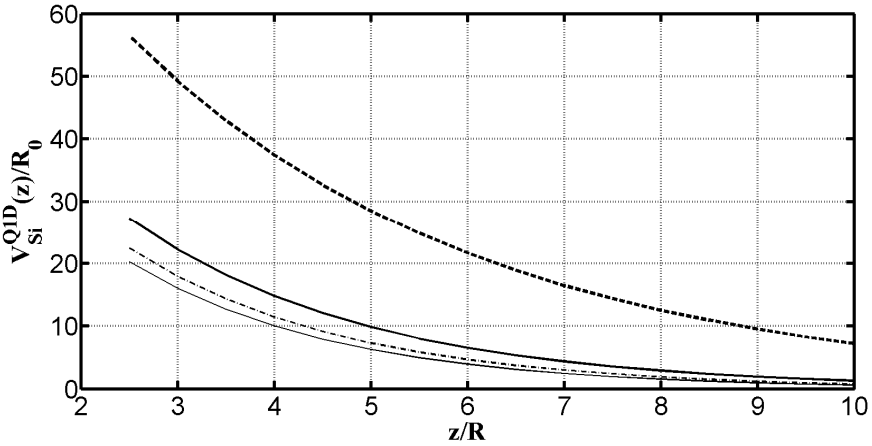

Fig.3. The screened exponential type interaction potential energy (scaled by the effective Rydberg R_0 =0.9 eV) as a function of intercharge longitudinal distance z (scaled by the QWR radius R=3 nm) for the different effective electron plasma density parameter values r_S and temperatures T. The thin solid and bold dashed curves show the screened potential energies for the r_{S1} = 0.0988 (n_{L1} = 1.1x10^{-6} cm^{-1}) at T = 4K and T = 17K with ε_{r1} = 23 , whereas the dashed-dotted and bold solid curves show the potential energies for the r_{S2}= 0.0494 (n_{21}= 2.2x10^{-6} cm^{-1}) at T = 4K and T = 17K with ε_{r2} = 11.5, respectively.

As follows, with "moderate" high density 1.1x10^{-6} cm^{-1} in the relatively narrow permitted thermal energy range SL enhances more than twice whereas for the high density 2.2x10^{-6} cm^{-1} an enhancement is rather 1.5 times but for the case when the permitted energy interval is 4 times larger. This indicates that with the linear density lowering, however, a temperature becomes a more dominant factor for SL. Now let us display the Q1D screened interaction energy numerical calculations for the QWR/barrier system on the base of PbSe active material.

In Fig. 3 we outline the screened exponential type interaction potential $V_{Si}^{Q1D}(z)$ as a function of the intercharge longitudinal distance z (scaled by QWr radius R) for the fixed temperature and linear density values. The highest (bold dashed) and lowest (thin solid) strongly separated graphical lines corresponds to the "moderately" high-density value n_{L1}=1.1x10^{-6} cm^{-1} at T = 17K and T = 4K respectively with the dielectric constant ratio ε_{r1} = 23. Nearly located two middle graphical lines (dashed dotted and bold solid) are corresponding to the high-density value n_{L2}=2.2x10^{-6} cm^{-1} with ε_{r2} = 11.5, where the top spaced line (bold solid) is relating to T=17K, while the low spaced line (dashed dotted) to the T = 4K, respectively. As shown, the energy graphical line (bold dashed) associated to the "moderately" high density n_{L1} = 1.1x10^{-6} cm^{-1} at T = 17K is enhanced more strongly than the corresponding line (bold solid) related to the twice as high density n_{L2} = 2.2x10^{-6} cm^{-1}. In turn, the screened effective potential energy lines at T = 4K are obviously weaker due to the comparatively large values $(q_S R)^2$.

4. Conclusions

In summary, by using the Thomas-Fermi method the proper model has been adopted for the description of the screening effect caused by quasi-one-dimensional electron gas in cylindrical quantum wire embedded in the barrier environment. In the *long wavelength moderate limit* for the moderately thin semiconductor QWr the screened Q1D interaction potential $V_S^{Q1D}(z)$ has been used such as

$$V_{Si}^{Q1D}(z) = -\frac{e^2}{\varepsilon_w R}\frac{1}{q_L R}e^{-q_L|z|} .$$

where $V_S^{Q1D}(z)$ depends on strongly both from the small screening parameter $q_L R$ and QWR radius R, indicating that the dielectric confinement effect enhances a strength of the screening potential as well as recovers and simultaneously modifies the effective screening length.

As shown, with the lowering of the linear density a temperature becomes a more dominant factor. It is found that in low temperature region the Q1D screening effect equalizes the DC effect when calculating the q_L^{-1}. In particular, at T=4 K despite an increasing of linear density two times and simultaneously decreasing of dielectric constant ratio twice takes place certain saturation of the SL due to the interplay between both the DC and Q1D screening effects related effective parameters. In the moderately high temperature region at T=77 K the DC effect play a key role in the formation of effective screening length value.

Calculated Q1D screened exponential type potential graphical lines are shown as a function of the intercharge longitudinal distance z along the wire axis for both the different fixed linear density and temperature values. As follows, with increasing of T an appreciable enhancement of calculated exponential potential $V_{Si}^{Q1D}(z)$ takes place in discussed cases when effective distance z < 5R. It has been obtained that the energy graphical line related to the "moderately" high density n_{L1} = 1.1x10^{-6} cm^{-1} with the dielectric constant ratio ε_r = 23 at T = 17K is enhanced more strongly than the corresponding curve related to the both twice as high density and twice as decreased ε_r .

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ELECTRICAL PROPERTIES OF PULSED LASER DEPOSITED p-InSb-n-CdTe HETEROJUNCTION

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1. Introduction

Indium antimonide (InSb) is an important material that is widely used in mid-infrared wavelength range photodetectors due to the unique electrophysical parameters and the narrowest band gap among of all A_3B_5 semiconductor compounds. Such photo-detectors have found wide applications in night vision devices, infrared systems,infrared spectroscopy and radiometry in order to obtain information from various objects and measure their temperature [1].

It is well known that the heterojunction (HJ) photodiodes have some advantages compared with homojunction photodiodesprimarily due to the presence of a "window" effect, which reduces the losses related to the surface recombination of carriers, the high resistance of layer and allows to have wider spectral sensitivity region. In this case an essential role is playing the coincidence of crystal structures and lattice constants of semiconductor HJ pairs for providing of these advantages. An ideal HJ could be formed between the InSb and cadmium telluride (CdTe). They both have a cubic crystal lattice and nearly perfect match of the lattice parameters (α_{InSb} = 6,479 Å, α_{CdTe} = 6,477 Å). The calculations show that the expected density of interface states at the HJ interface does not exceed the value of $N_s = 6.2 \times 10^{11}$ cm^{-2}. Therefore one can get close to the ideal junction which is characterized by a very low recombination rate for injected carriers at the interface. In addition one can note that the coefficients of thermal expansion of InSb ($\alpha_T = 4.9 \times 10^{-60}$ C^{-1}) and CdTe ($\alpha_T = (5.0\text{-}5.5) \times 10^{-60}$ C^{-1}) are also in a good agreement.

InSb based photodiodes usually can be fabricated by using impurity diffusion processes [2], ion implantation [3] followed by annealing, or by molecular beam epitaxy [4]. Alternative to the this methodsis a pulsed laser deposition (PLD) technology, which is widely recognized as a simple, but is a versatile method for depositing thin films and different structures [5,6]. Nowadays this technology allows us to obtain layers of ceramic materials, ferroelectric substances, oxides, superconductors, silicon carbide materials, nitrides, semiconductors, carbon, diamond-like carbon, fullerenes and polymers. The method is based on using physical phenomena that occurs with solid targets under the influenceof laser radiation. As a result of laser radiation spreading (ablation) of a substance from the irradiated zone of solid target to the substrate is observed. The method holds of unique characteristics:

1. Possibility of evaporation of practically all the materials including the one with high-melting temperature.
2. Short times of deposition (about 10^{-6} sec.), which is equivalent to improving the “effective vacuum” on a several orders.

In this paper, the InSb based HJ photodiodes were fabricated by depositing of n-CdTe layer on p-InSb substrate by PLD technique (assisted by Q-switched YAG: Nd^{3+} laser).The choice of technology is also motivated by the fact, that PLD allows an epitaxial film growth at rather low temperatures, which practically excludes the interdiffusion of semiconductor components during the growth process. Here we present the results of electrical characterisits of fabricated photodiodes.

2. Experiment

CdTe layers were grown by vacuum (3×10^{-5} mm Hg) PLD (1.064 μm wavelength, 30 ns pulse duration, energy 0.35 J and intensity of~10^8 W/cm^2 in the target irradiation zone) deposition from CdTe compound target onto factory quality p-type (acceptor concentration $N_A = 4.17 \times 10^{14}$ cm^{-3}) InSb substrate (thickness 400 μm) at the temperature of 300 °C. The thickness of deposited layer was determined from reflectance spectra (normal incidence of light) of fabricated (p)InSb-(n)CdTe structure by using thin-film measuring system Filmetrics F20 (fig. 1). The thickness of layer deposited from a single laser pulse was estimated by dividing layer thickness by a number of laser pulses, which was 4.7 nm per laser pulse. Low resistance contacts on both sides of HJ were formed after laser deposition of CdTe layer by thermal sputtering of indium (In). The contact layer covers the whole surface of the p-InSb substrate, while the diameter of partially covered area on n-CdTe layer is not more than 1 mm (depending on the junction area).

Dark current-voltage (I-V) and capacitance-voltage (C-V) characteristics of fabricated junctions have been carried out at liquid nitrogen temperature (~ 80K). The temperature dependence of the response of the photodiodes was studied as well.

3. Results and discussions

a) C-V characteristics

Fig. 2 shows $1/C^2$ dependence on the voltage for the HJ p-InSb-n-CdTe at 1 MHz frequency. The linearization of dependence C^{-2}-V with cut-off $V^C_{cut\ off}$= 0.42 V indicates the sharpness of impurity distribution in the space charge region, which is mainly located in p-InSb layer.

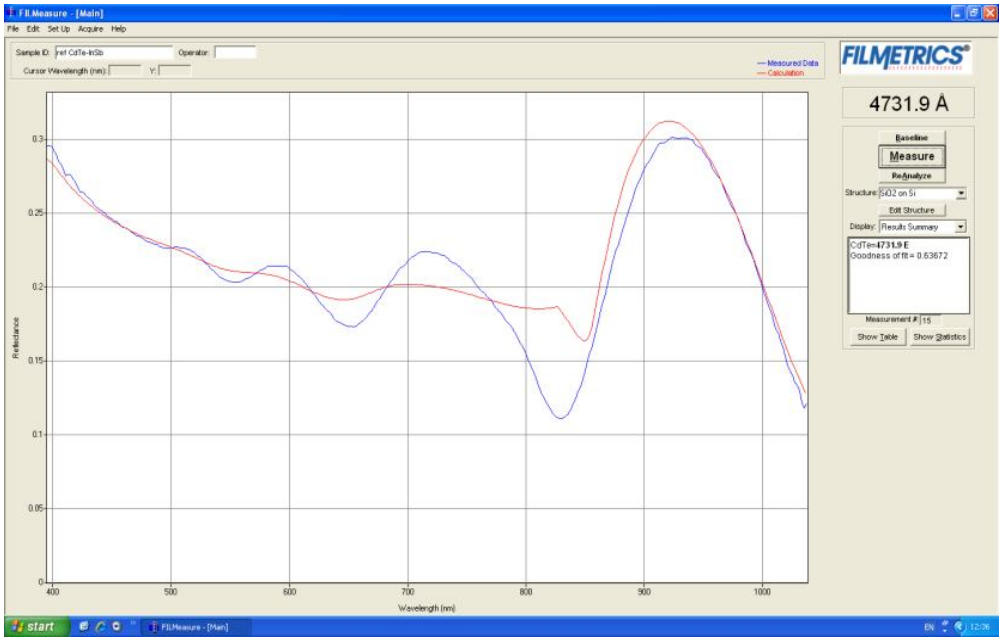

Fig. 1. Reflectance spectra (normal incidence of light) of (p)InSb-(n)CdTe structure (number of evaporating laser pulses is 100).

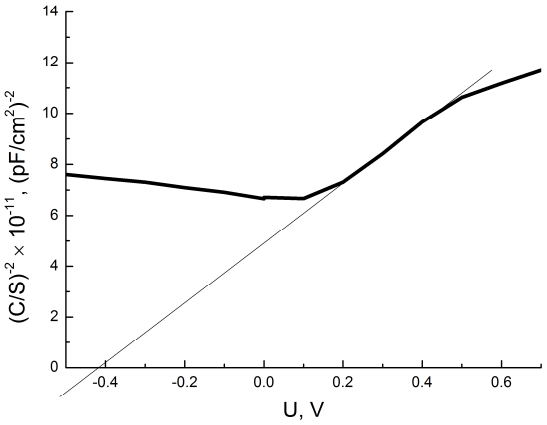

Fig. 2. $1/C^2$ dependence on applied voltage for the HJ p-InSb- n-CdTe.

b) I-Vcharacteristics

Fig. 3 shows dark I-V characteristics of the fabricatedp-InSb-n-CdTe photodiodes. For forward bias as we can see the current-voltage characteristics is linear for applied voltages higher than 0.5 V, $I = (V - V^I_{cutoff})/R$, where V^I_{cutoff}= 0.43 V, and R~ 32Ω is a residual differential resistance. For voltages less than 0.5 V, I-V characteristics can be explained by the power law of $I \sim V^{3/2}$. It is well known that such dependence can be found if the passage of currents is limited by the space charge due to the electron injection from a heavily doped CdTe layer into the quantum well formed in at the interface in InSb layer as a result of corresponding band edge offset and work function difference.

c) The response of the photodiode on thermal radiation.

We have measured the photoresponse of the heterostructure photodiode to the black body radiation emitted at different temperature. As a black body we have used the iron covered with white lacquer (ε_T=0.85 for infrared waves).

Figure 3 shows I-V characteristics of photodiode under black body radiation produced from heated material for several temperatures. As a measure for photoresponse, we took the short circuit current under illumination. We can observe that the potential barrier height for electrons to pass from CdTe to InSb is about 0.12 V.

The intensity of radiation on wavelength ranges from λ_1 to λ_2 is given by expression $R_T=\varepsilon_T\sigma T^4(z(\lambda_2/\lambda_m)-z(\lambda_1/\lambda_m))$, where

$$z(x) = \int_0^x \lambda^{-5}\left(e^{\frac{ch}{k\lambda T}}-1\right)^{-1} d\lambda \Big/ \int_0^\infty \lambda^{-5}\left(e^{\frac{ch}{k\lambda T}}-1\right)^{-1} d\lambda,$$

c is the speed of light, h - Plank's constant, k - Boltzmann's constant, λ –wavelength and T - absolute temperature [7]. The intensities of black body radiation reaching our photodiode in the spectral range of its sensitivity from (1μm to 5μm) are shown in table 1, where λ_m is the wavelength at the radiation maximum.

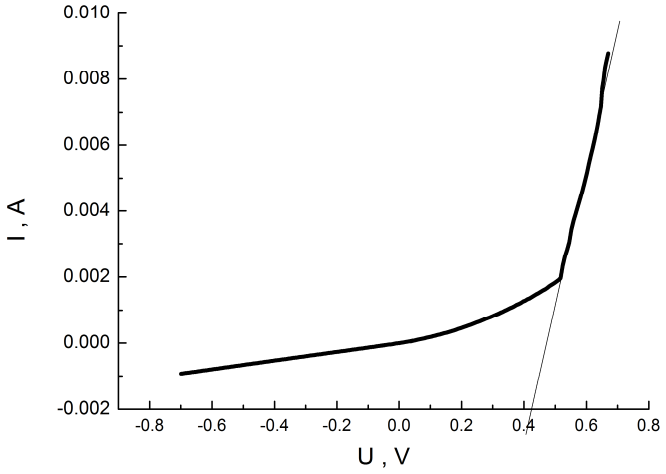

Fig. 3. Dark I-V characteristics of fabricated (p)InSb-(n)CdTe junction.

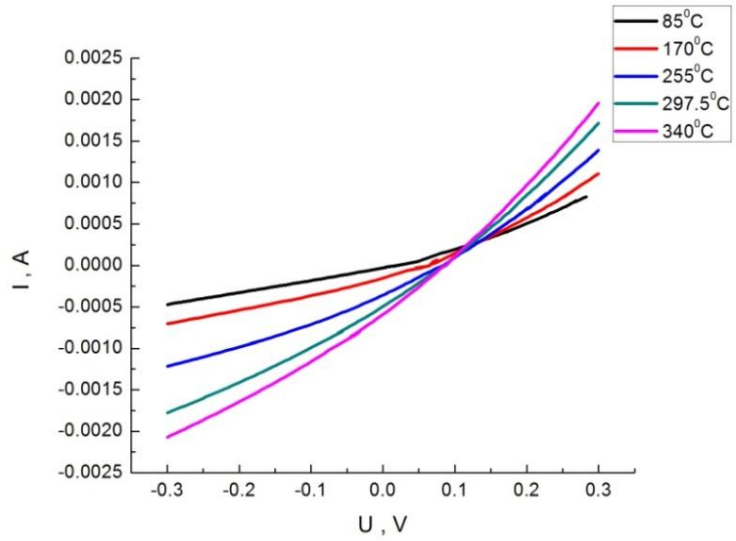

Fig. 4. I-V characteristics of fabricated p-InSb-n-CdTe heterojunction under black body radiation.

Temperature ^{0}C	Intensity W/cm^2	λ_{m}, μm	Photoresponse A
85	0.000382	8.09	3.17E-05
170	0.002472	6.54	0.00016
255	0.009124	5.49	0.00037
297.5	0.01411	5.24	0.000513
340	0.023977	4.73	0.000609

Table 1

4. Conclusion

p-InSb-n-CdTe heterojunctions have been fabricated by a simple low-temperature technology based on pulsed laser deposition (which eliminates the process of implantation, diffusion annealing). Photodiodes based on p-InSb-n-CdTe heterojunctions show good photoresponse and can serve as perspective detectors in the near and mid-infrared wavelength range.

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NANOSTRUCTURES GROWTH FEATURES IN $Ga_{1-x-y}In_xAl_yN$ QUASITERNARY MATERIAL SYSTEM

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1. Introduction

The most promising from the point of view of designing new materials and devices with unique properties is at present elaboration of technologies for creation of novel semiconductor nanostructures and study of their physical properties. Steadily increasing interest towards specifically semiconductor nanostructures is caused primarily by the existence of a wide spectrum of possibilities to control the properties of semiconductors. It is known that crucial changes in their properties may be achieved by varying the composition of semiconductor solid solutions, changing the concentration and type of impurities, changing external conditions and so on. Constraints of motion of charge carriers in one or more directions leading to the dimensional quantization phenomenon open additional possibilities of efficient control of properties of nanostructure-based devices by means of changing their sizes [1–4]. Modified density of states of quantum dots (QD), nanowires, and combined QD-nanopit structures leads to essential improvement of the working optoelectronic parameters of semiconductor devices, such as lasers, photodetectors, etc. Obviously, the electronic properties of QDs depend on dot structure and the mechanism of their formation. Such nanostructures can be fabricated by nanolithography or by the self-organization method (Stranski–Krastanov mode), which is at present the most frequently employed technique. Relaxation of elastic (deformation) strain as a principle of nucleation is the basic mechanism of formation of nanostructures in semiconductor materials such as Si, Ge, III–V compounds, etc.

GaN, InN, AlN and their ternaries and quaternaries alloys are considered as one of the important semiconductors. There are fabricated lighting and displayed application on the base of those materials. Particularly, GaInN alloys have recently attracted much attention as potential materials for fabrication of blue and green light emitted diodes (LEDs), as well as for violet and blue injection lasers. Since the band gap of GaInN can be varied from 2.0 to 3.5 eV by increasing GaN concentration, the potential operating wavelengths cover nearly the entire visible spectra range [5-8]. GaN is a promising material for use it in high-speed field effect transistors, high-temperature electronic devices, UV or blue light emitters, detectors and gas sensors [9]. It is known that InN has lowest effective mass and small band gap among all III-nitride semiconductors, which can allow to suggest that it can be used in light emitting devices and high speed electronic devices as well. In particular, by controlling indium composition, InN-related compounds, including $In_xGa_{1-x}N$ and $In_xAl_{1-x}N$, have been used for band-gap engineering, which have extended the emission of nitride-based light-emitting diodes from the UV to near infrared regions. InN also can be used in tandem solar cells and thermophotovoltaic systems [9]. In addition, the sufficient lattice mismatch between GaN/AlN, GaN/InN and InN/AlN equals to 3%, 10% and 12% respectively, allows considering those materials as very attractive also for nanostructures engineering in Stranski–Krastanov growth mode.

In this paper, the continuum elasticity model is applied to quantitatively investigate the growth features and nucleation mechanism of QDs, nanopits, and cooperative QDs–nanopits structures in GaInAlN quasiternary systems.

2. Calculation of total energy of cooperative QD-nanopit structures in GaInAlN material system

At the description of the competing nucleation mechanism, we assume that the surface has only discrete orientations and that only one angle needs to be considered [10], so GaInAlN-based QDs and nanopits have a shape as it is schematically presented in Fig.1.

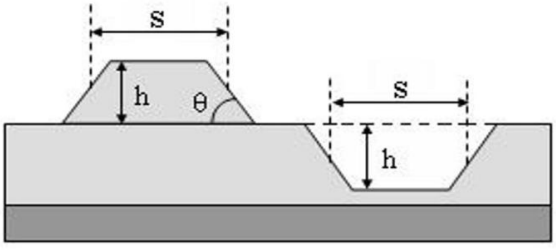

Fig. 1. Schematic view of the QD-nanopit structure's cross section.

The total free energy to form either a dot or a pit is $E = E_S + E_R$, where E_S and E_R are the change in surface free energy and the reduction of the strain energy by elastic relaxation, respectively. Minimizing the total free energy [10] with respect to

shape for fixed volume gives $s = t = h \times cot\theta$, where s, t, h and θ are the length, width, height (depth) and contact angle, as in Fig.1, the energy is equal to

$$E = 4\Gamma V^{2/3} Tan^{1/3}\theta - 6cV Tan\theta\,, \tag{1}$$

where $\Gamma = \gamma_e Csc\theta - \gamma_s Cot\theta$. For the crystals with a cubic symmetry $\gamma_s = \frac{1}{2}\cdot\varepsilon^2(C_{11}+C_{44})d_{wet}$, $c = \sigma_b^2\frac{(1-\nu)}{2\pi\mu}$, $\sigma_b = \varepsilon(C_{11}+C_{44})$. Here γ_s and γ_e are the surface free energy per unit area for the normal orientation and the beveled edge, respectively, $\varepsilon = \frac{\Delta a}{a}$ is the lattice mismatch ratio (strain) and d_{wet} is the wetting layer thickness. The value for γ_e can be found from Young equation $\gamma_{sl} = \gamma_s - \gamma_e Cos\theta$ [11], where for Stranski–Krastanov growth mode $\gamma_{sl} = 0$ is the surface free energy corresponding to the solid-liquid interface, $\nu = \frac{\lambda}{2(\lambda+\mu)}$ is the Poisson ratio, μ, λ and C_{ij} are the shear (Lame coefficients) and the elastic modulus of the substrate. Taking into account also dependence of the wetting layer thickness versus strain, the expression for the total energy can be written as

$$E = 4\left(\gamma_e Csc\theta - \frac{1}{2}\varepsilon^2(C_{11}+C_{44})a\cdot e^{-35.84\varepsilon}Cot\theta\right)V^{2/3}Tan^{1/3}\theta - 3\varepsilon^2(C_{11}+C_{44})^2\cdot\frac{(1-\nu)}{\pi\mu}\cdot V\,Tan\theta\,. \tag{2}$$

In order to obtain analytical expression for the strain (deformation) dependence of wetting layer thickness in the case of the GaInAlN quasiternary system, we performed mathematical approximation of experimental data. Approximation curves are presented in Fig. 2. We used in our calculations the following expressions for d_{wet}: in monolayers (ML): (i) if the deformation strain is positive, then $d_{wet} = 0.05\varepsilon^{-3/2}$ at $\varepsilon > 0.03$ [12] and $d_{wet} = 24.181e^{-31.034\varepsilon}$ at $0 < \varepsilon < 0.03$ (accuracy of approximation $R^2 = 0.9635$), (ii) if the deformation strain is negative, then $d_{wet} = 0.15|\varepsilon|^{-3/2}$ at $|\varepsilon| > 0.035$ [12] and $d_{wet} = 45.162e^{-23.03|\varepsilon|}$ at $0 < |\varepsilon| < 0.035$ (accuracy of approximation $R^2 = 0.9934$).

Dependence of the GaInAlN strain-induced dots and pits total energy versus volume, calculated at $\gamma_e = 10.15\cdot10^{-5}$ J/cm^2, $\mu = 30.34\cdot10^4$ J/cm^3, $C_{11} = 272.3\cdot10^3$ J/cm^3, $C_{44} = 130.3\cdot10^3$ J/cm^3, $\nu = 0.361$ and $\theta = 0.785$ (45°), is presented in Fig. 3(a) at different values of strain.

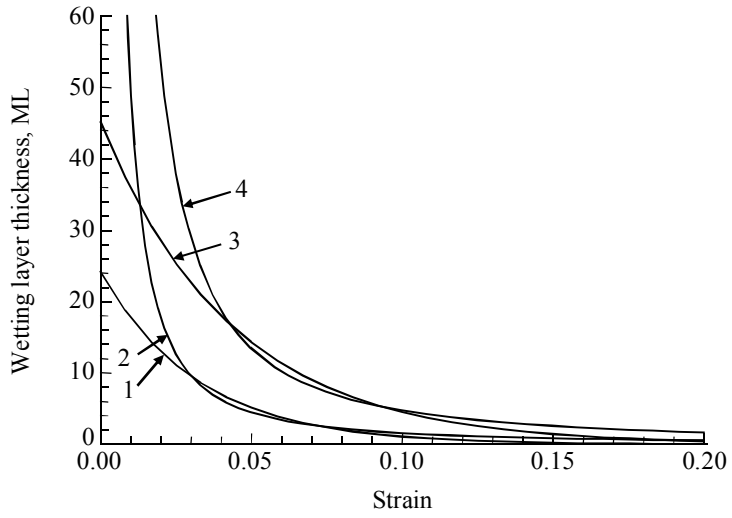

Fig. 2. Strain-dependence of the wetting layer thickness: (1) $d_{wet} = 24.181e^{-31.034\varepsilon}$ ML, $\varepsilon > 0$; (2) $d_{wet} = 0.05\varepsilon^{-3/2}$ ML, $\varepsilon > 0$; (3) $d_{wet} = 45.162e^{-23.03|\varepsilon|}$ ML, $\varepsilon < 0$; (4) $d_{wet} = 0.15|\varepsilon|^{-3/2}$ ML, $\varepsilon < 0$.

To attain a stable geometry, the island must first overcome the energy barrier E^* which occurs at volume V^*. Finding the maximum of (2), dependences of the critical energy and critical volume versus strain are presented in Figs. 3(b) and 3(c), respectively. From those figures is quite visible that both E^* and V^* strongly depend on the strain and dramatically decrease at the increasing of the strain, and at the critical strain of $\varepsilon^* = 0.039$ the sign of energy and volume is changed. We assume that at $\varepsilon = \varepsilon^*$ the mechanism of the nucleation is changed from the growth of dots to the nucleation of pits. Clearly, at small

misfit ($\varepsilon < \varepsilon^*$), the bulk nucleation mechanism dominates. However, at $\varepsilon > \varepsilon^*$, when the energy barrier becomes negative as well as a larger misfit provides a low-barrier path for the formation of dislocations, the nucleation of pits becomes energetically preferable.

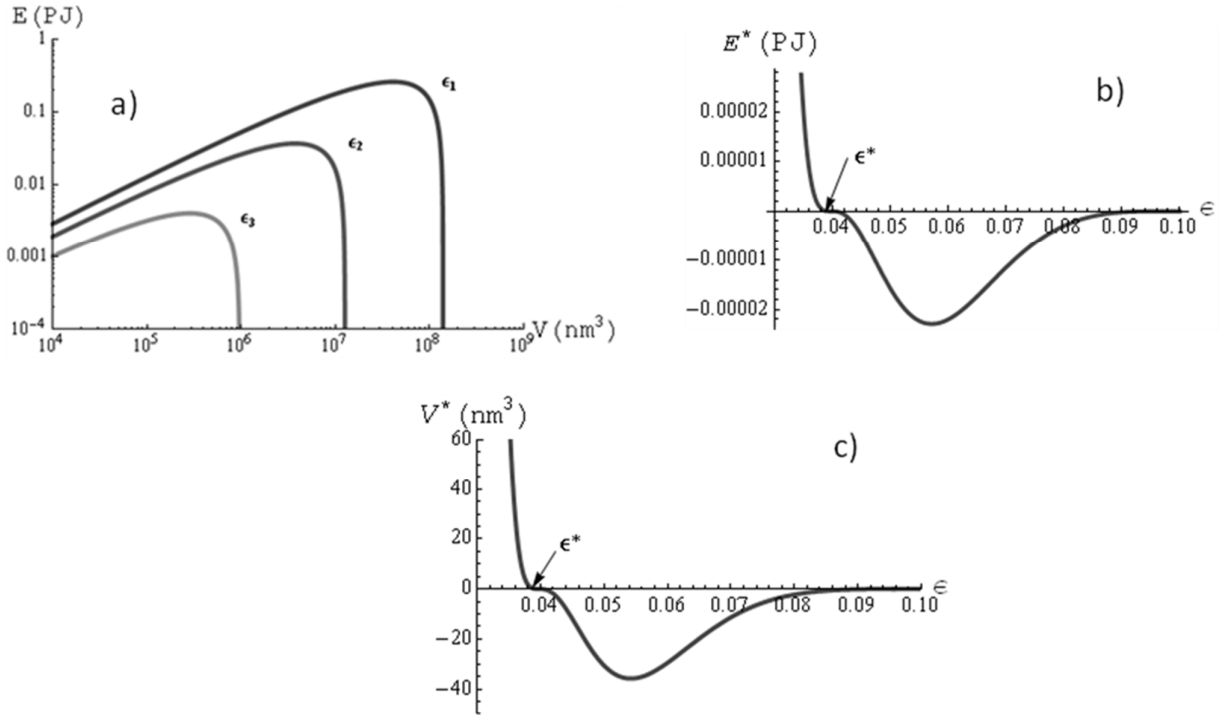

Fig. 3. (a) – dependence of the GaInAlN strain-induced islands (dots and pits) energy versus nanostructure's volume at different strain (1 – ε_1=0.02, 2 – ε_2=0.025, 3 – ε_3=0.03). Critical energy – (b) and critical volume – (c) versus strain.

3. Conclusions

Thus, the continuum elasticity model was applied to quantitatively investigate the growth features and nucleation mechanism of QDs, nanopits, and cooperative QDs–nanopits structures in GaInAlN quasiternary systems. It was shown, that nanostructures formation critical energy (E^*) and critical volume (V^*) strongly depend on the strain and dramatically decrease at the increasing of the strain. Calculations revealed that for GaInAlN material system at the critical strain of ε^* = 0.039 the sign of critical energy and volume is changed. We assume that at $\varepsilon = \varepsilon^*$ the mechanism of the nucleation is changed from the growth of quantum dots to the nucleation of nanopits. Obviously, at small misfit ($\varepsilon < \varepsilon^*$), the bulk nucleation mechanism dominates. However, at $\varepsilon > \varepsilon^*$, when the energy barrier becomes negative as well as a larger misfit provides a low-barrier path for the formation of dislocations, the nucleation of pits becomes energetically preferable. Presented results are very important from technological point of view and can be used at nanoengineering in GaInAlN material system.

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SPECIFIC FEATURES OF THE ELECTRONIC STATES IN A CYLINDRICAL NANOLAYER WITH ADDITIONAL LONGITUDINAL POTENTIAL AND THE QUANTUM MECHANICAL ASSESSMENT OF SAMPLE'S GEOMETRIC CHARACTERISTICS

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1. Introduction

Recently a growing interest is observed in studies of the physical properties of two-dimensional electron gas on a curved surface of a semiconductor in models like quantum cylinder, quantum sphere and nanotubes of different geometry. In addition, experiments have been conducted on faceted surfaces of GaAs/GaAlAs structures containing two-dimensional electron gas (see e.g. [1-5]).

In most theoretical works devoted to studies of the physical properties of cylindrical nanolayers usually, from the very beginning, it is assumed that the charge carriers are localized on the surface of nanolayers (see e.g. [3-5]) and by this the finiteness of sample's thickness is neglected. While describing a wide range of phenomena, this approach is mostly justified, but as a result, the unique properties of a quantum cylinder are being lost (i.e. the properties combining the distinctive physical features of both a quantum wire and quantum film [6]).

Another aspect of above series of works is that the additional potential resulting with the growth of nanostructure is usually modeled either by straight barrier [4,5] (going along the cylinder), or by an extended spiral δ - barrier. As a result, the actually existing spatial expansion of the potential barrier is being neglected.

In present paper, we consider a more realistic model of a circular tube sector. This model allows us to take into account both a) the finiteness of the cylinder's thickness and b) the spatial expansion of the barrier passing along the generitrix of the cylinder.

It was also established an explicit correspondence between the geometrical and quantum-mechanical characteristics of the nanolayer.

2. Research methods

In a nanotube with cross section shown in Figure 1 the motion of electrons is free along the axis of the tube but at the same time it is limited simultaneously in radial and azimuthal directions. In this case, one can represent the limiting potential in the following form

$$U(\rho,\phi,z)=U(\rho)+U(\phi), \tag{1}$$

where $U(\rho)$ is the radial potential (modeled by Vulcano potential [7], and $U(\varphi)$ is the azimuthal potential (modeled by the potential of infinitely deep well).

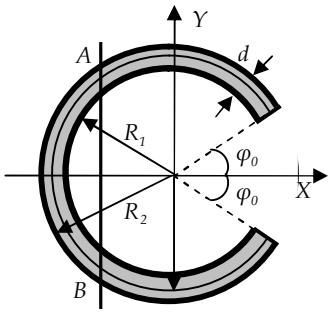

Fig. 1. The cross section of the nanotube

By solving the Schrödinger equations and using the obvious boundary conditions, we obtain the following expressions for the wave function and energy spectrum of the electrons

$$\Psi(\rho,\varphi,z)=\psi(\rho)\Phi(\varphi\ )\sqrt{1/L}\,exp(ikz),$$

where

$$\psi(\rho)=\psi_{n,M}(\rho)=C(n,M)\left(\frac{\rho^2}{2\Delta^2}\right)^{\frac{M}{2}}exp\left(-\frac{\rho^2}{4\Delta^2}\right)L_n^M\left(\frac{\rho^2}{2\Delta^2}\right), \tag{2}$$

$$\Phi(\varphi\ )=\frac{1}{\sqrt{\pi-\ \varphi_0}}\cdot\begin{cases}sin\dfrac{\pi m(\pi-\varphi\ )}{2(\pi-\ \varphi_0)}, & m=\pm2,\pm4,\cdots\\ cos\dfrac{\pi m(\pi-\varphi\ )}{2(\pi-\ \varphi_0)}, & m=\pm1,\pm3,\cdots\end{cases}, \tag{3}$$

$$E=E^{\perp}(n,m)=\frac{\hbar^2}{2m^*\Delta^2}\left(2n+1-\frac{1}{2}\left(\frac{\rho_0}{\Delta}\right)^2+\sqrt{\frac{1}{4}\left(\frac{\rho_0}{\Delta}\right)^4+\frac{\pi^2m^2}{4(\pi-\ \phi_0)^2}}\right). \tag{4}$$

Here the following notation are introduced: $C(n,M)=1/\Delta\sqrt{\Gamma(M+n+1)n!}$ is the coefficient of normalization and $L_n^{\beta}(x)$ are generalized Lager polynomials,

$M=\sqrt{\beta^2+\frac{\pi^2m^2}{4(\pi-\phi_0)^2}}=\sqrt{\beta^2+\frac{m^2}{4(1-\gamma)^2}}$, $\phi_0=\pi\gamma$, $(0\le\gamma<1)$, $\beta=\frac{\rho_0^2}{2\Delta^2}$ and $E_{n.m}^{\perp}$ is the energy of the electron's transverse motion.

As can be seen from the formula (4) and Figure 2, the electrons' energy spectrum consists of series produced by superposition o the energies of azimuthal and radial motions.

From formula (4), in the limiting case when the condition

$$\varepsilon_1/\varepsilon_2\propto\left(l\ /\Delta\right)^2>>1, \tag{5}$$

is fulfilled for the energy, we'll have

$$E=E^{\perp}(n,m)=\varepsilon_1(2n+1)+\varepsilon_2m^2. \tag{6}$$

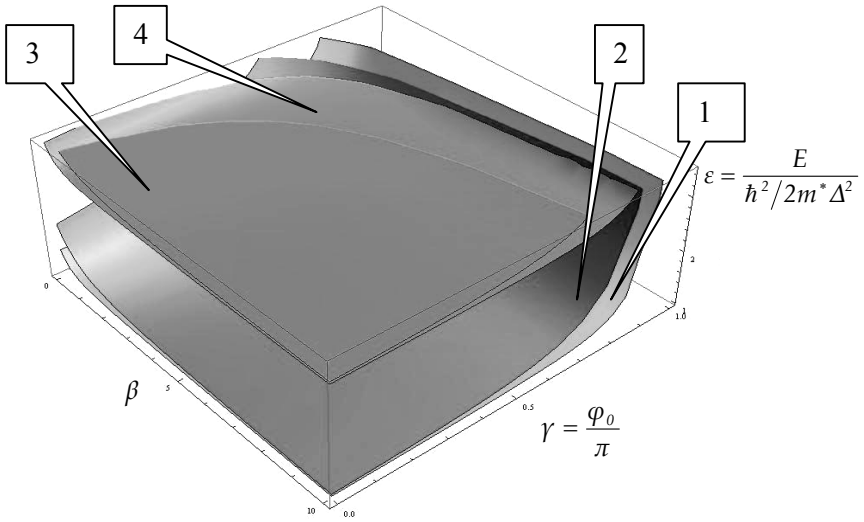

Fig. 2. The dependence of dimensionless energy $\varepsilon=E\Big/\frac{\hbar^2}{2m^*\Delta^2}$ from the parameters of γ and β, for various values of quantum numbers n and m. 1- $(n=0,m=\pm1)$; 2- $(n=0,m=\pm2)$; 3- $(n=1,m=\pm2)$; 4- $(n=1,m=\pm1)$;

In Eq. (5) we introduced the following notations: $\varepsilon_1=\hbar^2/2m^*\Delta^2$ and $\varepsilon_2=\hbar^2\pi^2/2m^*l^2$ (where $\varepsilon_1,\varepsilon_2$ are the quanta of energy in the radial and azimuthal directions, respectively and $l_\varphi=2(\pi-\varphi_0)\rho_0$ is the length of the field localization in the azimuthal direction). In this case, the radial quantization levels are the basic ones and the azimuthal quantization levels are the satellites. It is easy to see that when the reverse condition of (5) takes place, for the energy of the electron again the expression (6) is obtained, but in this case the base and satellite levels are reversed.

3. The geometrical parameters and the quantum-mechanical characteristics of the nanosystem

It is generally accepted that the thickness of the nanolayer matches with the width of the classically allowed region of electrons' motion (see e.g. [7]), i.e. it is determined by the equation $E_F=U(\rho)$ (E_F is Fermi energy), but this approach to our opinion is inconsistent.

Indeed, the above condition is true only in the quasi-classical region where the quantum numbers n and m obtain sufficiently big values. Since for big values of n and m a lot of size-quantized sub-bands are being filled, the size effects virtually disappear.

On the other hand, since the Fermi energy depends on the concentration and energy spectrum of the electrons, the effective geometrical characteristics of the nanosystem determine also the wave functions of the quasiparticles.

For definiteness let's consider the ground state $(n=0)$, for the distribution function of which from (2) we have

$$P(x)=\frac{2}{\Gamma(M+1)}x^{2M+1}\,exp\left(-x^2\right), \tag{7}$$

where $x=\sqrt{2}\rho/2\Delta$. Obviously, the effective radius and the thickness of the nanostructure may be described by mathematical expectation $R_0=\overline{\rho}=\langle 0|\rho|0\rangle$ and dispersion $\sigma=\left(\langle n|\rho^2|n\rangle-\left(\langle n|\rho|n\rangle\right)^2\right)^{\frac{1}{2}}$ of the distribution function (7), for which we will have

$$R_0=\overline{\rho}=\langle 0|\rho|0\rangle=2^{\frac{1}{2}}\Delta\frac{\Gamma\left(M+\frac{3}{2}\right)}{\Gamma(M+1)},\qquad \sigma=\sqrt{2}\Delta\sqrt{\left(\frac{\Gamma(M+2)}{\Gamma(M+1)}-\left(\frac{\Gamma\left(M+\frac{3}{2}\right)}{\Gamma(M+1)}\right)^2\right)}. \tag{8}$$

Figure 3 shows a graph of dependence $R_0=\overline{\rho}=\langle 0|\rho|0\rangle$ from the β parameter, in $\sqrt{2}\Delta$ units.

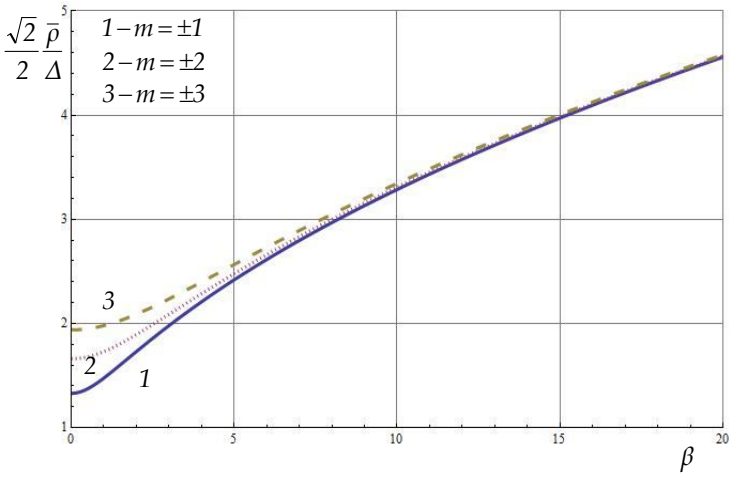

Fig. 3. The dependence of $\frac{\sqrt{2}}{2}\frac{\overline{\rho}}{\Delta}$ from the parameter β for $m=\pm1,\pm2,\pm3$ and $\varphi_0=\pi/2$.

Figure 4 shows a graph of dependence of $\sigma=\left(\langle n|\rho^2|n\rangle-\left(\langle n|\rho|n\rangle\right)^2\right)^{\frac{1}{2}}$ from the β parameter, in $\sqrt{2}\Delta$ units.

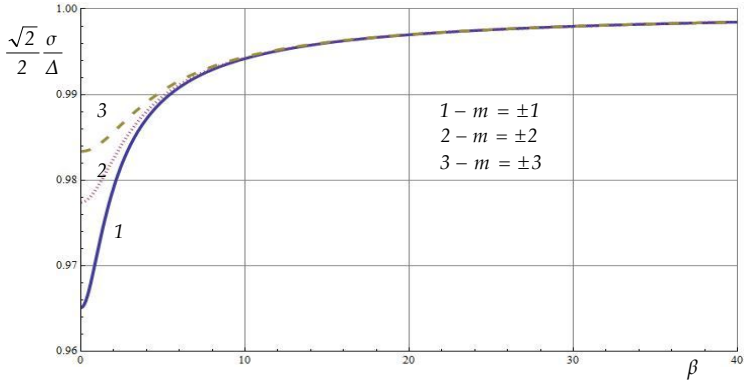

Fig. 4. The dependence of $\frac{\sqrt{2}}{2}\frac{\sigma}{\Delta}$ from the parameter β for $m=\pm1,\pm2,\pm3$ and $\phi_0=\pi/2$.

In the specific case of a thin layer ($M>>1$) from (8) we obtain

$$R_{01}=\rho_0,\ \sigma=\sqrt{2}\Delta/2$$

Formulas (8) allow us to determine the sizes of the nanolayer (see Fig. 1)

$$R_1 = R_0 - \eta\sigma\,, \qquad R_2 = R_0 + \eta\sigma\,, \qquad d = R_2 - R_1 = 2\eta\sigma\,, \tag{10}$$

Here η is an adjustable parameter, which can be conveniently represented in the form $\eta = [R_0/\sigma]$ ($[x]$ is the integer part of the quantity x).

Table 1 shows the numerical values of these quantities at different values of the parameter β

By knowing the geometric characteristics of the nanolayer R_1, R_2 and φ_0 and using the above numerical values, it is possible to solve the inverse problem as well. Bearing in mind that

$$R_1 = \widetilde{R}_0\Delta - 2\widetilde{\sigma}\Delta, \quad R_2 = \widetilde{R}_0\Delta + 2\widetilde{\sigma}\Delta.$$

Table1. The dependence of nanolayer's geometrical characteristics and the probability of particle's existence within the nanolayer from the parameter β ($\phi_0 = \pi/12$, $m = \pm 1$, $\eta = 2$)

β	0..01	0.1	1	10	100
$\widetilde{R}_0 = R_0/\Delta$	1.148	1.152	1.38	3.281	10.038
$\widetilde{\sigma} = \sigma/\Delta$	0.477	0.477	0.484	0.497	0.5
$\widetilde{R}_1 = R_1/\Delta$	2.102	2.106	2.348	4.275	11.038
$\widetilde{R}_2 = R_2/\Delta$	0.194	0.198	0.412	2.287	9.038
$\widetilde{d} = d/\Delta$	1.908	1.908	1.936	1.988	2
Probability	0.962	0.961	0.959	0.955	0.955

We will obtain a system of equations

$$\begin{cases} \dfrac{R_1}{R_2} = \dfrac{\widetilde{R}_0 - 2\widetilde{\sigma}}{\widetilde{R}_0 + 2\widetilde{\sigma}}\,: \\ R_2 - R_1 = 4\widetilde{\sigma}\Delta \end{cases} \tag{10}$$

Solving (10) by taking in account (8) and (9) one can find the parameters β and Δ of the wave function and thereby explicitly define the wave functions of the electrons.

As a conclusion, the developed method allows describing the electronic states and establishing un ambiguous relationship between the microscopic and macroscopic properties of the system.

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THE STUDY OF DOUBLE AND TRIPLE LAYER GRAPHENE INTERFACE BY SPECTROSCOPIC RAMAN MAPPING

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The transition from bi- to triple layer graphene, synthesized by micromechanical exfoliation, has been investigated by Raman mapping. Raman maps of 2D and G peaks show that the changes in the intensity, position and FWHM of the peaks are connected with the increase of the number of the layer and not with the disorder or strain in graphene.

1. Introduction

Graphite is a highly anisotropic material made of weakly coupled layers of carbon atoms bonded in a hexagonal lattice. Its building block, an isolated single atomic layer (monolayer) called graphene, could be accessed experimentally [1-4]. The electronic properties change dramatically for the monolayer graphene as compared to few layers and the bulk graphite. As graphene is a new nano-material with unusual electronic properties, its electronic, optical, thermal and other properties have not been studied completely yet [5-8]. Raman spectral imaging (or mapping) is a method for generating detailed images based on a sample's Raman spectrum [10-12]. Raman mapping has proved to be a basic tool to gain insight into the composition of artworks' multilayered structures, is sensitive to material concentration, phase, stress/strain, and crystallite. The aim of the paper is to investigate the bi/triple layer graphene system, synthesized by micromechanical exfoliation, by Raman mapping and clarify if the changes obtained are connected with the change of the number of the layers of graphene.

2. Experiment

Graphene samples are synthesized by Scotch tape method, identified by optical microscopy, and then characterized by Raman spectroscopy (spectra and mapping). The thickness of SiO_2 on the top of Si substrate is 300 nm. The Raman spectra are measured by WITec Alpha300 Raman system (spectral resolution of spectrometer is 1 cm^{-1}) using a laser excitation of 514.5 nm delivered through a single-mode optical fiber. Using a long working distance focusing objective lenses (10x and 100x) with a numerical apertures NA = 0.90 and 0.80 a spot size of ~ 500 nm is obtained. With an incident light power of 0.2 mW heating effects can be neglected. The Raman spectra are measured using a grating with 1800 g/mm and a solid state cooled CCD detector. The Raman spectra and mapping of as-prepared graphene samples are recorded under the same experimental conditions. Typical acquisition times for such maps can be in the order of 1-10 sec per point (or longer), and thus total measurement times can be significant.

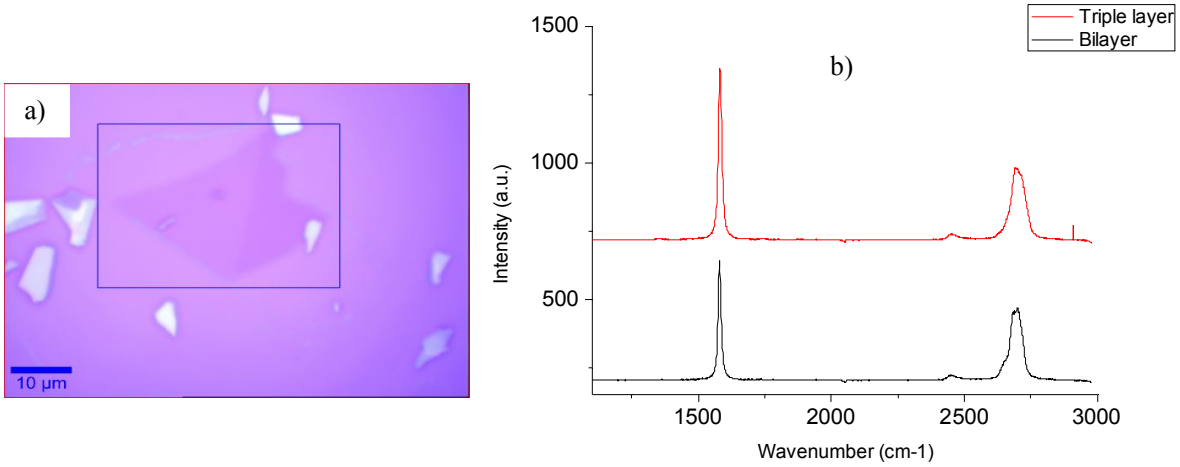

Fig. 1. Optical micrograph of Raman mapping area (a) and Raman spectra of bi- and triple layer graphene at excitation wavelength of 514 nm (b).

3. Results and Discussion

Raman spectra of bi- and triple layer graphene and Raman mapping for 2D and G peaks are investigated. Fig. 1 shows an optical micrograph and Raman spectra of a sample composed of a varying number of layers (double and triple) of graphene, respectively. Raman spectra, i.e. the shape and the position of the 2D and G peaks (Fig. 2) confirm that the sample is

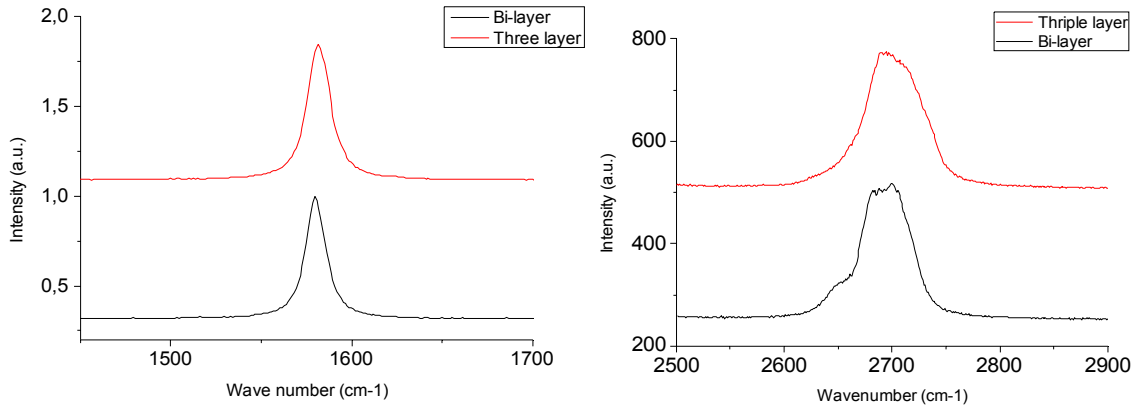

Fig. 2. G (a) and 2D (b) peaks of bi- and triple layer graphene at excitation wavelength of 514 nm.

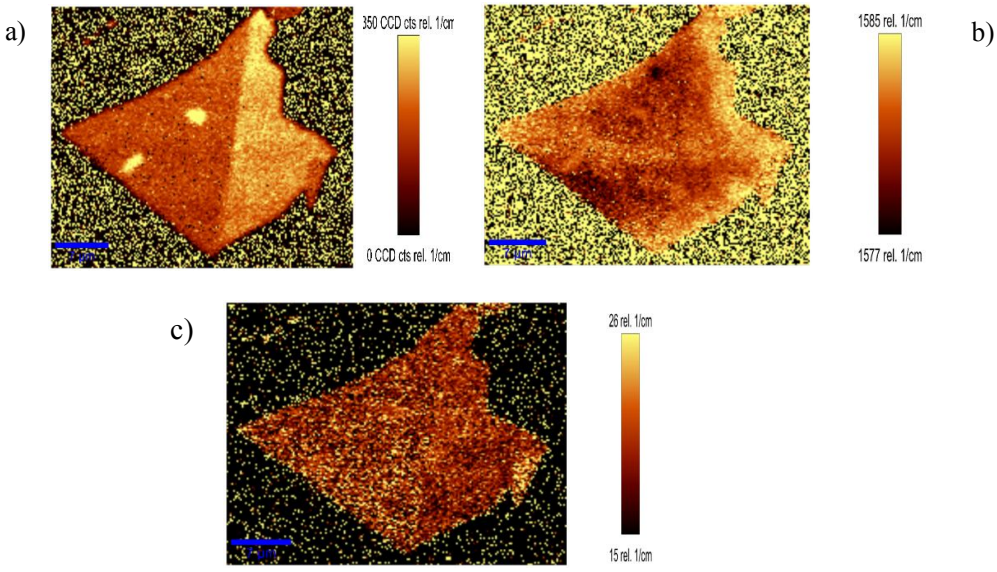

Fig. 3. Intensity (a), position (b) and FWHM (c) of G peak of bi- and triple layer graphene.

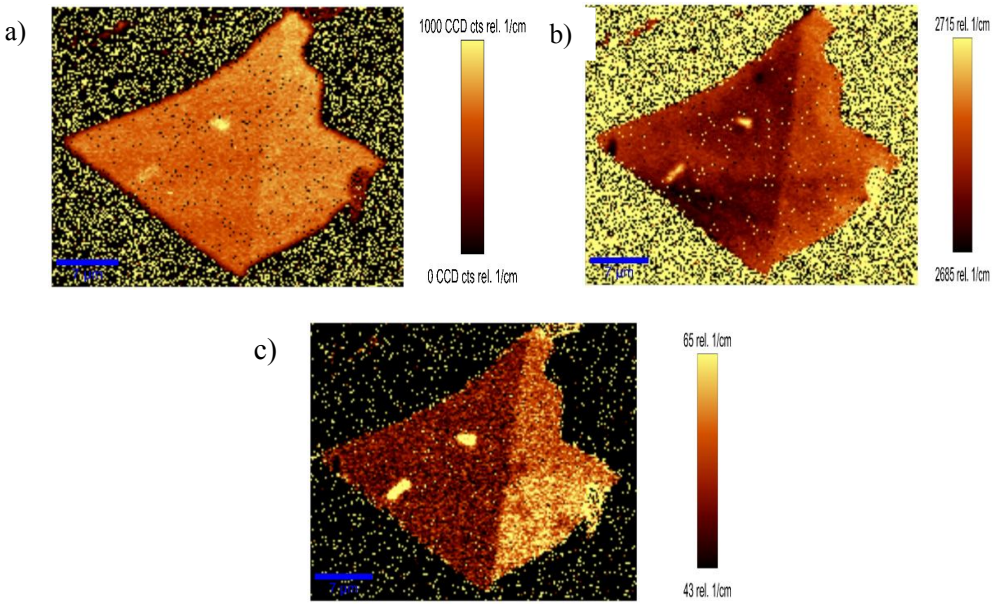

Fig. 4. Intensity (a), position (b) and FWHM (c) of 2D peak bi- and three layer graphene.

composed partly of double and triple layer graphene. Analyses of Raman spectra showed that 2D band spectral shape is strongly dependent on graphene thickness (Fig. 2) and G band position is changing with the number of layers in graphene (Fig. 2). The Raman maps of G (Fig. 3) and 2D peaks (Fig. 4) are investigated to clarify if the changes of the position and FWHM are connected with disorder or strain in graphene or just because of the increase of the number of layers of graphene.

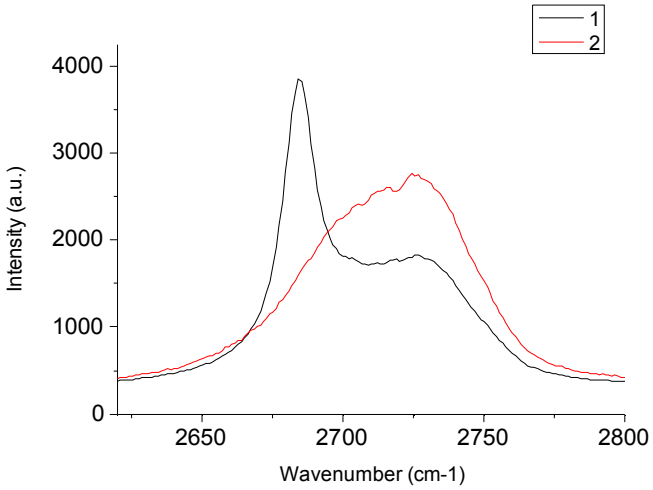

Fig. 5. Raman spectra of 2D peak taken from the transition of mono (a) /double (b) layer grapheme.

Analysis of the intensities, positions and FWHM of bi- and triple layer graphene system show that the integrated G line intensity is increased with the number of layers, FWHM and the position of G peak (Fig. 3) are almost the same at the transition from double to triple layer. The mapping of the 2D line indicates that the integrated intensity of monolayer graphene is high, but for few and multilayer it keeps constant and FWHM is increased (Fig. 4). A large FWHM of G peak, together with position of G peak close to 1580 cm^{-1} and no D peak, fingerprint the most intrinsic samples.
Thus, Raman mapping was performed to obtain information on film uniformity, as well as to investigate directly the transition from a double to a triple layer. Besides, we clarified that the laser spot size is very important during investigation. If the spot size is directed, i.e. on the interface of mono- and double layers.
It is possible to catch both mono- and few layer lines on Raman spectra (Fig. 5).

4. Summary

The Raman spectra and mapping show that the changes in the intensity, position and FWHM of the peaks are connected with the increased number of graphene layers and not with the disorder of graphene. Besides, Raman spectra show that 2D peak strongly depends on number of layers, which allow us to differentiate mono- from bilayer or bi-layer from triple graphene from multilayer ones.

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SCREENED COULOMB CENTERS IN LEAD SALT/MESOPOROUS SILICA SBA 15 PHASE REALISTIC SEMICONDUCTOR QUANTUM WIRE SYSTEM

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1. Introduction

The energy spectrum and other physical characteristics of Coulomb centers (impurities and excitons) in quasi-one-dimensional (Q1D) semiconductor quantum wires (QWr) surrounded by the low dielectric constant barrier environment are under intensive investigations. These nanosystems are favorable because in addition to dimensional quantization effects, which make an exciton or impurity center Q1D, image potentials due to the large contrast between dielectric constants of the semiconductor and dielectric barrier environment also play an important role [1]. They notably intensify the attraction between the charges in Coulomb pair (dielectric confinement effect (DC effect)), hence enhancing both the exciton binding energy and interbank transition oscillator strength [1, 2]. In this point of view the lead salt binary compound semiconductor nanowire system inside the channels of mesoporous silica SBA-15 represents considerable interest owing to extremely distinguish QWR/barrier dielectric constants contrast ($\varepsilon_w \sim 17 \div 50$ and $\varepsilon_b \sim 1.4 \div 2.1$) as well as highly ordered and uniform mesoporosity of barrier media [3]. The most interesting experimental data of lead salt/mesoporous silica semiconductor quantum wire system are connected with the luminescence for that a massive blue shift is observed in related spectra. The latter clearly shows the presence of the quantum size effects in these systems and, therefore, to a great extent may be affected by excitons [3].

Quasi-free carriers in these systems may screen the Coulomb interactions between charge carriers and, in turn, the influence of screening produced by free carriers in Q1D structure is considerably weaker than in 3D or 2D semiconductor systems [4]. In this paper we investigate the screened excitonic bound state energy properties of semiconductor QWr enhanced due to the DC effect.

2. Theory

Let consider infinitely long semiconductor cylindrical QWr of radius R filled by semiconductor material with the dielectric constant ε_w and embedded in the dielectric barrier environment with the dielectric constant ε_b. A QWr contains a Q1D EG where the electrons there are confined to move in a QWR and are free to move along the axis of the wire by mean linear density n_L. Moreover, a strong confinement regime is accepted in discussing case, assuming that the quantum wire radius R is small compared with the Bohr radius a_0 in the semiconductor bulk samples ($a_0 >> R$). For that case the large asymptotic distances between the interacting particles along the wire axis $|z| >> R$ are essential. As shown in [5], the tunability of the Coulomb interaction in the QWr due to the DC effect enhances and modifies the Q1D screening potential. As result, in the intermediate distance range for a cylindrical wire $R < |z| \sim q_L^{-1}$ the interaction potential depends exponentially on interparticle distance z

$$V_S^{Q1D}(z) = -\frac{e^2}{\varepsilon_w R}\frac{1}{q_L R}e^{-q_L|z|} \quad . \tag{1}$$

In (1) R is the QWr radius, $q_L = \sqrt{q_S^2 + q_d^2}$, $q_d = (1/R)\sqrt{2/\varepsilon_r \ln \varepsilon_r}$, $\varepsilon_r = \varepsilon_w/\varepsilon_b >> 1$ (the DC effect condition). Here $q_S^{-2} = R^2[(\pi^2/32 r_S) + (K_1/16)\sqrt{\pi x} + (r_S x/4) + (K_2 x/4K_3)][(1/r_S) + (4/K_3)\sqrt{x/\pi}]^{-1}$ [4] with $K1 \approx 14.91$, $K_2 \approx -15.61$, $K_3 \approx -0.38$, $x = k_B T/R_0$, $k_B T$ is the thermal energy, $R_0 = \hbar^2/2m_w a_0^2$ is the bulk effective Rydberg, $r_S = (2a_0 n_L)^{-1/2}$ is the 1D spacing of free carriers in the units of Bohr radius $a_0 = \varepsilon_w \hbar^2/m_w e^2$.

Now we interested to find the screened excitonic bound states energy levels in the potential (1). For that, we shall solve the Schrödinger wave equation

$$-\frac{\hbar^2}{2m_w}\frac{d^2\psi}{dz^2} + V_S^{Q1D}(z)\psi = E\psi \quad . \tag{2}$$

As follows, Eq. (2) does not change under reflection $z \to -z$, therefore in accordance with the standard treatment of 1D problem [12] the solutions $\psi(z)$ must possess both even and odd parity. We look for bound state solutions of wave equation (2) and thus introduce proper substitutions for that case such as [12]: $E = -\hbar^2\chi^2/2m_w$, $y = \xi \exp(-q_L|z|)$, $\xi = \sqrt{8m_w E_R/q_L^2\hbar^2}$, $E_R = e^2/\varepsilon_w R q_L R$, $\nu = 2\chi/q_L (\chi > 0)$. Afterwards Eq. (2) takes the Bessel equation form

$$\frac{d^2\psi}{dy^2} + \frac{1}{y}\frac{d\psi}{dy} + (1 - \frac{\nu^2}{y^2})\psi = 0 \ . \tag{3}$$

Because $\psi(x)$ must decrease as $z \to \infty$ ($y \to 0$) then we have the solution of Eq. (3) in the standard form

$$\psi(x) = C\,J_\nu(x) = C\,J_\nu[\xi \exp(-q_L z)] \ . \tag{4}$$

The eigenvalues of the system at the origin $z \to 0$ are defined by the conditions of

$$\frac{d}{dz} J_\nu[\xi \exp(-q_L z)]\Big|_{x=0} = 0 \,, \tag{5}$$

$$J_\nu[\xi \exp(-q_L z)]\big|_{x=0} = 0 \,. \tag{6}$$

for both the even and odd states respectively. Eqs. (5) and (6) give the screened exciton energy eigenvalues of the system for the given mean linear density n_L, permitted reduced temperature parameter x and QWr radius R, which we will get numerically in the next section. In particular, from Eq. (5) we calculate the enhanced ground-state energy, namely, the screened exciton binding energy graphical dependence versus R and compare with the unscreened exciton counterpart. On purpose to give more comprehensive analytical description of the problem and for comparison as well, we develop the variational method for calculating both the binding energy and dimension of a quasi-one-dimensional exciton confined in a QWr inside a bulk dielectric media. Unlike the former technique, this approach makes possible to receive the analytical expressions for the screened exciton binding energy and 1D extent of wave function around exciton (exciton 1D mean length) in QWr.

The standard variational principle deals with the functional

$$E[\phi] = \int \phi^*[H_{kin} + V_S^{Q1D}]\,\phi dV \ , \tag{7}$$

where the average value over $|\psi(z)|^2$ of the screened potential $<V_S^{Q1D}(z)>$ should be used. According to the strong confinement regime, the normalized one parameter trial wave function of the exciton ground state is chosen as

$$\psi(z) = \sqrt{1/L}\sqrt{\lambda/2}\exp(-\lambda z/2) \,, \tag{8}$$

where λ is the variational parameter, L is the wire length. After necessary standard calculations both the variation parameter and the screened exciton ground state binding energy are obtained in the below form

$$\lambda = \left(\frac{2}{a_0 R^2}\right)^{1/3} \lambda_{q_L,R} \ , \tag{9}$$

$$E_b(q_L,R) = -\frac{e^2}{\varepsilon_w R}\frac{1}{q_L R}\left[\left[1 + q_L R\left(\frac{a_{ex}}{R}\right)\right]^{-1} - \frac{q_L R}{8}\frac{a_0}{a_{ex}}\frac{R}{a_{ex}}\right]. \tag{10}$$

In Expression (9)

$$\lambda_{q_L,R} = \sqrt{1 + \left(\frac{q_L R}{3}\right)^3 \frac{a_0}{2R} + \sqrt{1 + 2\left(\frac{q_L R}{3}\right)^3 \frac{a_0}{2R}}} + \sqrt{1 + \left(\frac{q_L R}{3}\right)^3 \frac{a_0}{2R} + \sqrt{1 + 2\left(\frac{q_L R}{3}\right)^3 \frac{a_0}{2R}}} \ .$$

In accordance with the functional choice in Exp.(8) the inverse variation parameter $(\lambda/2)^{-1} = a_{ex}$ determines the screened exciton 1D mean "length" in QWr with the DC effect such as

$$a_{ex}(q_L,R) = \left(a_0 R^2/2\right)^{1/3} (2/\lambda_{q_L,R}) \,. \tag{11}$$

Exp. (11) for the screened exciton "length" corresponds, in accordance with Exp.(10), to the intermediate interparticle distance range for the "moderately" thick wires, defined as

$$q_L R\, a_{ex} < R < a_0 \,. \tag{12}$$

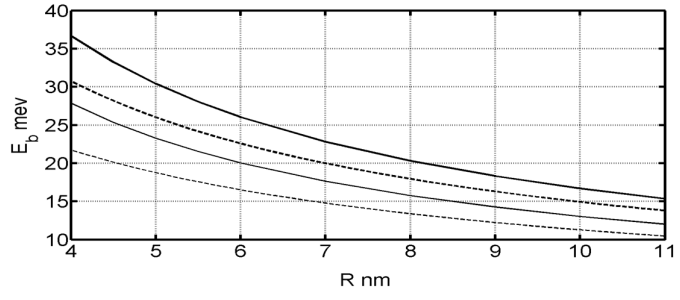

Fig.1. The binding energy of the screened exciton as the function of QWr radius R for the fixed linear density ($n_L \approx 1.5\cdot10^{-6}$ cm^{-1}) and temperature (T ≈ 26 K).

3. Numerical calculation

In order to display numerically the screened Coulomb properties we refer to the model with the PbSe based QWR embedded in the mesoporous silica SBA-15 barrier environment. Accordingly, the following material parameters are adopted: $m_w \approx 0.0355 m_0$ (m_0 is the free electron mass) and $\varepsilon_w \approx 23$ [23], which leads to $a_0 \approx$ 34.45 nm and $R_0 \approx$ 0.91 meV parameter values. With the $\varepsilon_b = 2$ [1] we have the dielectric constants ratio value $\varepsilon_r = 11.5$. For the

numerical analysis of q_S^{-2} the moderately high linear density $n_{L1} \approx 1.5 \cdot 10^{-6}$ cm^{-1} and the moderately low temperature $T \approx 26$ K values are taken into consideration. For that case the DC effect responsible term $q_d R$ exceeds just 1.5 times the screening effect counterpart $q_S R$ in $q_L R$, indicating that these contributions are in the same order. In Fig. 1 we outline the graphical results of screened exciton binding energy as a function of the "moderately" thick (see Eq. (12)) QWr radius R in accordance with Exps. (5) and (10). The received graphical lines are shown in compare with the QWr unscreened potential graphical curves ($q_S \to 0$). The top two solid and solid-dashed bold lines corresponds to the unscreened potential case both for the Bessel and variational equations (Eqs. 3, 5), respectively. While the low standing two thin solid and solid-dashed lines corresponds to the screened potential case (Eq. (1)) for the foregoing equations, respectively. As follows, in "moderately" thick QWr with the DC effect, the screened exciton binding energy is seen to exceed the bulk effective Bohr energy $R_0 \approx$ 0.91 meV by more than one orders of magnitude. In Table 1 we present the binding energy $E_b(q_L, R)$ calculations results when QWr radius decreases from $R_1 \approx 10$ nm to $R_2 \approx 5$ nm. As we can see both from the graph and

Method	Variation				Bessel equation			
$R_{1(2)}$=10(5)nm	E_{b1}	E_{b2}	E_{b2}/E_{b1}	$E_{b2} - E_{b1}$	E_{b1}	E_{b2}	E_{b2}/E_{b1}	$E_{b2} - E_{b1}$
Unscreened	14.9	23.3	1.56	8.4	16.7	33.4	2.0	16.7
Screened	11.3	18.8	1.66	7.5	13	23.3	1.8	10.3

Table 1. The numerical results of binding energy E_b for the QWr radius $R_{1(2)}$=10(5) nm with the fixed linear density ($n_L \approx 1.5 \cdot 10^{-6}$ cm^{-1}) and temperature ($T \approx 26$ K).

table, numerical results the screening effect reduces essentially screened DC effect enhanced exciton binding energy E_b and the latter is more effective for the small values of R in the permitted radius range in accordance with Exp. (12). Nevertheless, the screened exciton E_b values are enough enhanced due to the DC effect that even for the "moderately" thick QWr radius value R=10nm they will support distinguish stability in exciton pair. Note, that the Bessel equation wave function type calculations overestimate the E_b values in relation to the variation equation Coulomb type wave functions (corresponding graphical curves are enhanced more strongly), but, meanwhile, the E_b modifying rate is almost the same for both methods.

4. Conclusions

In summary, by using both the Bessel equation and variational methods formalism for studying the screened exciton states in lead salt/mesoporous silica SBA 15 phase realistic semiconductor QWr system is developed theoretically. For the "moderately thick" QWr the problem of screened exciton binding energy E_b has been investigated both analytically and numerically. The strong enhancement of the E_b (~ $20 \div 30$ meV) in comparison with the unscreened bulk value (~ 0.9 meV) is received in the presence of the exponential- the types of potential, demonstrating that quantum and dielectric confinement overbalance together to the Q1D screening effect. The allowed intervals of Q1D screened exciton E_b in correlation with QWr radius are also established.

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SUBSTRATE TEMPERATURE EFFECTS ON STRUCTURAL AND OPTICAL PROPERTIES OF CdS THIN FILMS DEPOSITED BY VACUUM FLASH EVAPORATION TECHNIQUE

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1. Introduction

Cadmium sulfide (CdS) is a common material used in the formation of solar cells based on cadmium telluride (CdTe) and $CuInGaSe_2$(CIGS). In such solar devices n-type CdS thin-film acts as optical window due to high bandgap energy Eg=2.42eV. For solar cells application CdS films have to have relatively high conductivity (>10^{16} cm^{-3}) to reduce electrical loses of solar cells, thin thickness to provide high transmission and good uniformity in order to prevent electrical short-circuit effect. The structural, optical and electrical properties of CdS thin films strongly depend on the applied technique and the substrate temperature [1]. Different techniques have been reported for the deposition of CdS thin films namely: vacuum evaporation [2], spray paralysis [3], electro-deposition [4] and chemical path deposition [5]. Among these vacuum evaporation technique is a well established technique for the preparation of uniform films. In this technique in contrast to many other techniques during the process of film depositionthe substrate is not heated that allow to deposit films at low temperatures. Due to this feature, vacuum evaporation technique is applicable for formation of solar cells on flexible poly-imide substrate. Replacing the glass substrate to a flexible polyimide substrate reduces the weight of thin film solar cells by 98%. Such solar cells are very promising for application on spacecraft so far as they have high ratio of electric power to weight. Flexible solar cells represent also of interest in the market for the terrestrial applications as they can easily be mounted on the surface of various shapes.

For fabrication of solar cell on flexible polyimide substrates, it is necessary to use low-temperature film deposition techniques because polyimide substrates do not allow heating more than 400^0C. As such techniques the most promising are the magnetron sputtering method and the method of the physical vacuum evaporation such as flash evaporation and thermal evaporation. Flash evaporation technique is most applicable for deposition of thin films of multicomponent alloys whose constituents have different vapor pressures (particularly CdS) because provides the stoichiometric composition of deposited films.

The aim of this work was to study the structural and optical characteristics of the CdS thin films deposited on the glass substrates by flash evaporation technique.

2. Experimental details

Thin films of CdS were fabricated by flash evaporation technique on commercial glass slides used as substrate with thickness of 1 mm and diameter 20 mm. The substrates were thoroughly cleaned by soap-free detergent ultrasonically and then iteratively rinsing in distilled water to remove the traces of detergent. Thereafter the substrates were cleaned ultrasonically in ethanol and then dried by blowing air. The vacuum chamber was pumped to a base pressure of $1.5x10^{-5}$ Torr before evaporation.

Schematic view of flash evaporation setup is presented in Fig. 1. The starting material was pure crystal of CdS which is pounded to a powder with particle dimensions of 50 –150 μm and then placed inside a batcher.

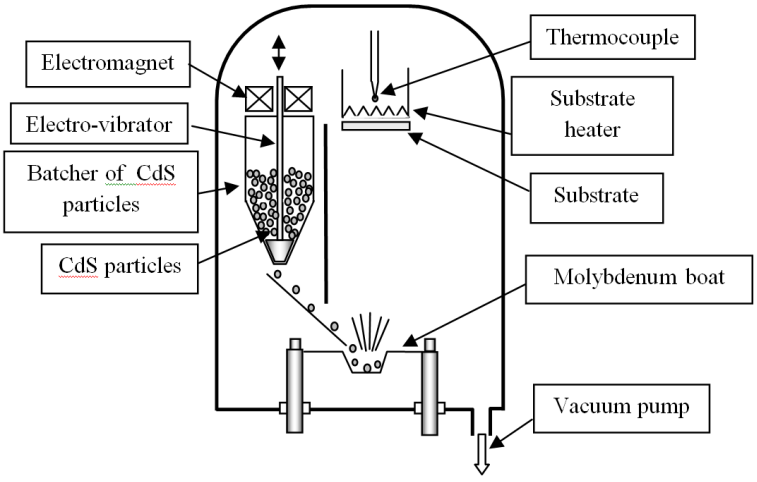

Fig.1. Schematic representation of the experimental setup.

Dispensing the CdS particles from batcher onto the molybdenum boat was performed due to opening and closing of batcher outlet by the instrumentality of electro-vibrator (Fig. 1).

The amount of CdS particles falling into the boat was controlled by opening time of outlet. The outlet is opened when electro-vibrator attracts up by electromagnet. In our experiments, the opening time was varied from 0.2 to 0.5 s. The outlet is opened again for evaporation of a next new portion of CdS particles only after evaporation of all particles contained in the boat.The evaporation process monitored through the chamber's window.

Dispensing the CdS particles was started afterthe boat is heated up to temperature 1200^0C - 1300^0C suitable to evaporate the CdS powder. The distance between the boat and substrate was about 12 cm.

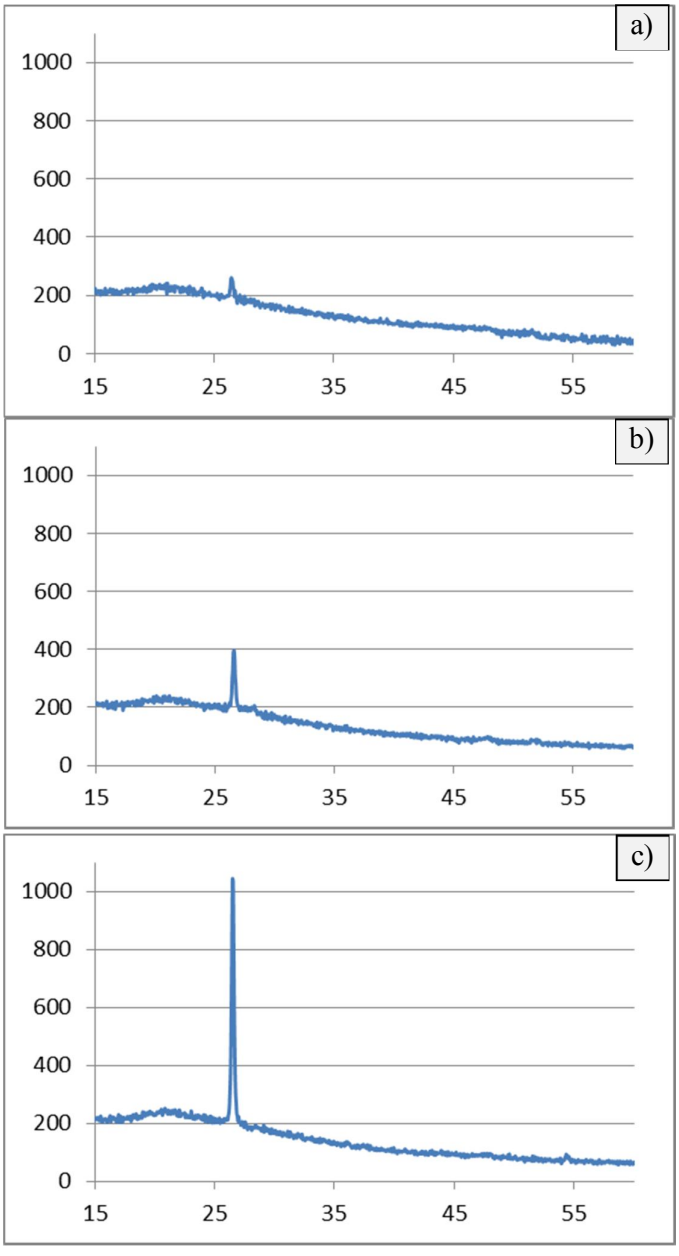

Fig. 2. XRD patterns of CdS films deposited at substrate temperature:a) 300^0C, b) 200^0C, c) 100^0C.

Distinguishing feature of this method is that the small particles of multicomponent alloy (in our case it is CdS binary semiconductor) whose constituents (Cd and S) have different vapor pressures fall from vibrator into the preheated boat and at each moment in the boat there are particles with different temperatures which are at different stages of evaporation. The presence of large quantity of particles in the boat which are at different stages of evaporation provides at the average the same fluxes of evaporated constituents (Cd and S) and provides the stoichiometric composition of deposited film with pinpoint accuracy.

The film thickness and the duration of deposition were typically 300-600 nm and 20-40 min. The CdS films were deposited at substrate temperatures of 100^0C, 200^0C and 300^0C. The structural properties of samples were studied by X-ray diffractometer URD-6 in the θ-2θ mode using Cu - K_α(λ = 1.5405 Å) radiation. The surface roughness and thickness of films were investigated by ZYGO profiler. Transmittance and reflectance, over the wavelength from 400 to 1000 nm were measured using double beam Filmetrics F20 spectrophotometer.

3. Results and Discussion

3.1. Structural properties of CdS thin films deposited at different substrate temperatures

Figure 2 shows the X-ray diffraction patterns of the CdS thin films deposited by flash evaporation technique on a glass substrate at 100^0C, 200^0C and 300^0C temperatures. Diffraction patterns were recorded over the 2θ range from 150 to 750 with the step 0.10. XRD analyses showed that the CdS films were polycrystalline. All CdS films exhibit a predominant sharp peak at 2θ around 26.50 which can be assigned to either the (002) plane in the case of hexagonal structure [JCPDS card no: 41-1049] or the (111) plane in the case of cubic structure [JCPDS card no: 10-0454].

The exact interpretation of XRD patterns is quite difficult because most peaks of cubic and hexagonal CdS structure differ negligible within the very small angle.

The summery of XRD data of as-deposited CdS thin films at different substrate temperature are presented in Table 1.

It is seen from Table 1 that observed interplanar spacing-d and diffraction peaks in the XRD patterns when 2θ =26.518^0 (substrate temperature 100^0C), 2θ =26.591^0, 2θ =51.577^0 (substrate temperature 200^0C),2θ = 26.473^0, 2θ =51.546^0(substrate temperature 300^0C) correspond with reflection from the crystal planes (002), (112) of CdS hexagonal structure, which agrees well with standard XRD patterns (JCPDS card no: 41-1049).

It is seen from Fig. 2 that the intensities of diffraction peak (002) increase with a decrease of the substrate temperature.

Lattice parameter (c) was evaluated from the highest intensities of diffraction peak (002) [6]. It is seen that the observed values are in good agreement with the standard data (Table 1).

The structural parameters of CdS thin films such as the average grain sizes (D), dislocation density (δ), the number of crystallites per unit area (N) and micro-strain (ε) are presented in Table 2.

The average grain sizes (D) of the film was calculated using the Scherrer's equation [7]: $D = 0.9\lambda/\beta\cos(\theta)$, where λ is the wavelength of the X-ray used (λ=1.5405 Å), β is the full-width at half-maximum (FWHM) of the (002) peak which has maximum intensity, and (θ) is the Bragg's angle.

The variation of the grain size with substrate temperature is presented in Table 2. It is seen from Table 2 that the grain size vary insignificantly and the biggest grain size observed at 200^0C of substrate temperature.

Table 1. XRD data of as-deposited CdS thin films at different substrate temperatures

Substrate temperature	2θ, (^{0})	d (Å) observed from XRD	d (Å) standard JCPDS	[hkl] plane	c(Å) observed values	c(Å) standard JCPDS
T=100^0C	26.518	3.3614	3.3567	002	6.7228	6.7134
T=200^0C	26.591	3.3523	3.3567	002	6.7046	6.7134
	51.577	1.7721	1,761	112	x	x
T=300^0C	26.473	3.3670	3.3567	002	6.734	6.7134
	51.546	1.7731	1,761	112	x	x

Table 2. Structural parameters of as-deposited CdS thin films at different substrate temperature calculated from 002 peaks.

Substrate temperature	2θ, (^{0})	FWHM (deg)	D (nm) from XRD results	[hkl] plane	δ 10^{15} lines/m^2	ε x10^{-4}	N x10^{15} m^{-2}	Thickness of films (nm)(t)
T=100^0C	26.518	0.35	29.49	002	1.15	11.8	8.576	220
T=200^0C	26.591	0.35	30.43	002	1.08	11.4	8.514	240
T=300^0C	26.473	0.35	28.95	002	1.2	12	12.353	300

The dislocation density δ defined as the length of dislocation lines per unit volume, has been calculated using the equation [8]: δ=1/D2. The results of calculation are presented in Table 2. The small values of (δ) confirmed the good crystallinity of the CdS films. The number of crystallites per unit area (N) and the micro-strain (ε) of the films have been estimated with the use of the following equations [9]: N=t/D3 and ε=β cos(θ)/4. It is seen from Table 2 that the lower values of micro-strains and the number of crystallites per unit area observed at 200^0C of substrate temperature. The lower values of micro-strain indicate that the lowest concentration of lattice imperfection correspond to the substrate temperature 200^0C.

3.2. Optical properties of CdS thin films deposited at different substrate temperatures

The transmission and reflection spectrum of CdS thin films measured in the spectral range 400 - 1000nm. Using transmittance (T) and reflectance (R) spectra the absorption coefficient has been calculated by the following equation:

$$\alpha = \frac{1}{t}\ln\frac{1-R}{T},$$

where *t* is the thickness of CdS film.

Above the fundamental absorption edge the dependence of the absorption coefficient on the incident photon energy is given by Tauc's model [10]:

$$\alpha h\nu = B\left(h\nu - E_g\right)^n,$$

where *hν* is the photon energy, E_g is the optical bandgap, and *B* is a constant and *n* is an exponent that depends on the type of optical transitions. For direct allowed transitions $n = ½$. The variation of $(\alpha h\nu)^2$ of CdS thin films deposited at different

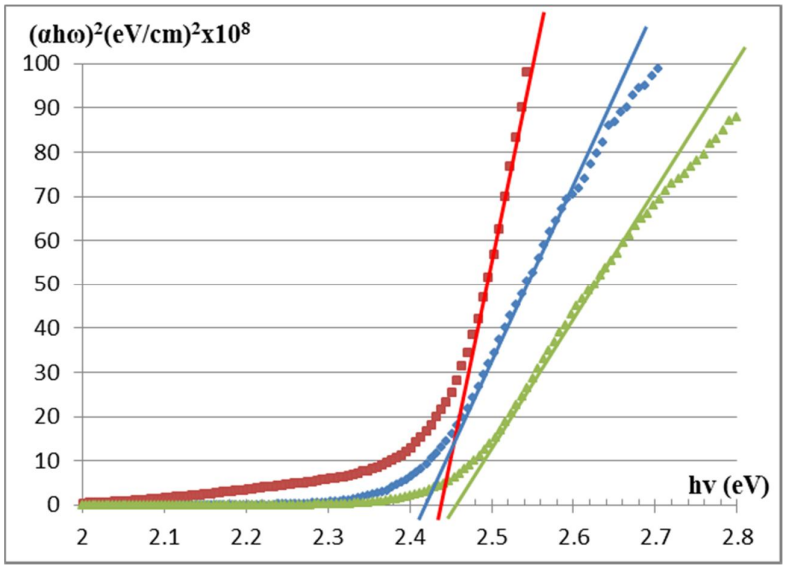

Fig. 3. Plots of $(\alpha\cdot h\nu)^2$ vs. photon energy (hν) of the CdS thin films deposited at substrate temperature: a) 300^0C, b) 200^0C, c) 100^0C.

substrate temperatures as a function of photon energy are shown in Fig. 3.

Using the liner extrapolation method the value of the optical bandgap is determined to be 2.43eV, 2.42eV and 2.41eV for 100^0C, 200^0C and 300^0C, accordingly. The results of measurements have shown that the CdS thin film deposited at 200^0C have the same optical bandgap as the bulk of CdS crystal.

4. Conclusion

The structural and optical properties of the CdS thin films deposited on glass substrate at different temperatures (100^0C, 200^0C and 300^0C) by vacuum flash evaporation technique have been investigated. XRD results showed that the CdS thin films were polycrystalline and all films have hexagonal structure and exhibit a predominant sharp (002) peak at 2θ around 26.5^0. It is found that the intensities of diffraction peak (002) increase with a decrease of the substrate temperature.

Using XRD results the structural parameters of CdS thin films such as the average grain sizes (D), dislocation density (δ), the number of crystallites per unit area (N) and micro-strain (ε) was calculated. These results have shown that the CdS thin films with the best crystalline structure obtained at substrate temperature of 200^0C.

The results of optical measurements have shown that the CdS thin films deposited at different temperatures have optical bangaps slightly differ from each other. The optical bandgap typical for bulk of CdS crystal was observed for CdS thin film deposited at 200^0C.

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THE NATURE OF OPTICAL TRANSITION IN THE CdS_xSe_{1-x} SEMICONDUCTOR NANOCRYSTALS

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1. Introduction

Semiconductor nanoparticles have been studied extensively for a quarter century due to their potential applications in semiconductor lasers, nonlinear optical devices, photovoltaic cell, thin film transistors, display devices and gas sensors [1-3]. Nanometer-sized crystals have distinctive optical properties due to the confinement of charged particles in all three dimensions. The bandgap can be modified to optimize the optical properties of the nanostructure by controlling its size. CdS_xSe_{1-x} semiconductor nanocrystals in glass have been most widely studied in a model system for quantum-confinement effects trough optical methods [4,5]. In this work, we analyze the nature of optical transition in the CdS_xSe_{1-x} semiconductor nanocrystals, which are in different stages of formation.

2. Experiment

The CdS_xSe_{1-x} nanocrystals in silicate glass were fabricated using the procedure of [6]. The samples differ from each other by mean sizes of nanocrystals and degrees of perfection of crystal lattice. The formation of semiconducting nanocrystals corresponded to a thermal treatment temperature of 530^0C. The temperature of the heat treatment is reached over one hour, then the samples are stored at a constanat temperature (sample T_1 is not thermally processed and the processing times of samples T_2 –T_8 at a temperature of 530^0C are t_2=5 min, t_3=15 min,t_4=35 min, t_5=65 min, t_6=125 min, t_7=245 min and t_8=425 min). The transmission spectra studied in the wavelength interval 300-900 nm using Ocean optics USB-4000 spectrometers.

On the spectral dependence of the absorption coefficient can distinguish the fundamental absorption region, which corresponds to electron excitation from the valance to conduction bands . The fundamental absorption region can be used to determine the nature and value of the optical band gap (E_g). The optical band gap has been calculated using Tauc's formula [7]

$$(\alpha h\nu)^{1/m} = A(h\nu - E_g)\,, \qquad (1)$$

where α-is the absorption coefficient, $h\nu$ is the incident photon energy, A is a constant dependent on the nature of the optical transition, and m indicates the nature of optical transition in the material. For bulk semiconductors the value of m is $1/2, 2, 3/2,$ and 3 corresponding to the allowed direct, allowed indirect, forbidden direct and forbidden indirect transitions [7], respectively. As CdS_xSe_{1-x} is a direct band gap material, m = ½ for the allowed transition. The band gaps has been calculated by extrapolating the linear region of the plots $(\alpha h\nu)^2$ vs $h\nu$. In samples that are in the initial stage of formation is not always possible to select a linear region that makes it difficult to determine the value of the energy gap. In such samples, E_g can be determined from the relationship $\frac{d\{\ln(h\nu)\}}{d(h\nu)}$ vs $h\nu$. Now Eq. (1) can be written as follows:

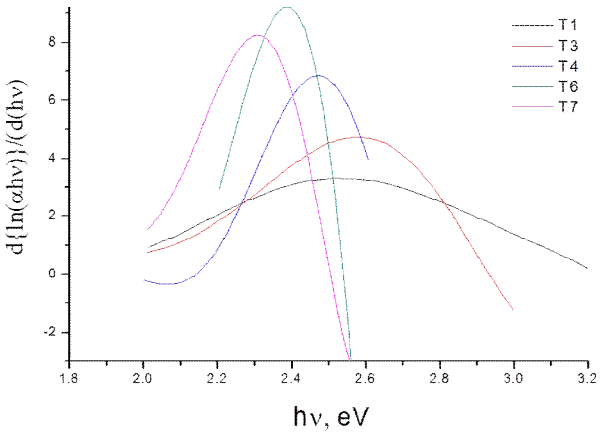

Fig. 1. Plot of $\frac{d\{\ln(\alpha h\nu)\}}{d(h\nu)}$ vs. $h\nu$.

$$\frac{d\{\ln(\alpha h\nu)\}}{d(h\nu)} = \frac{m}{(h\nu - E_g)}: \qquad (2)$$

So, there should be a discontinuity in $\frac{d\{\ln(\alpha h\nu)\}}{d(h\nu)}$ vs $h\nu$ plot at the bandgap energy. In fact, the value of the bandgap energy can be considered energy $h\nu$ in which dependence $\frac{d\{\ln(\alpha h\nu)\}}{d(h\nu)}$ vs $h\nu$ is a maximum. In order to construct the mentioned plot, dependence $\ln(\alpha h\nu) = f(h\nu)$ was fitted to polynomial form. Further, the mathematical equation describing the de-

pendence is derived by $h\nu$. A few examples depending $\frac{d\{\ln(\alpha h\nu)\}}{d(h\nu)}$ vs $h\nu$ are shown in Fig. 1. It is seen that maximum is relatively weak at the initial stage of the annealing, which can be due to the absence of the perfect crystal lattice. When the heat treatment time increases the degree of perfection of the lattice increases and the maximum becomes more expressed. Fig. 2 shows the dependence of the bandgap, which were determining two different ways vs. heat treatment time. As can be seen the value of bandgap are close enough. Reducing the value of the band gap of the heat treatment time is due to the increasing size of the nanocrystals. The dependence of the coefficient m from the incident photon energy contains important information about changes in the nature of the optical transitions in nanocrystals. Using the value of bandgap energy, we can determine the value of m. Again, from Eq. (2) we can get

$$\ln(\alpha h\nu) = lnA + m\ln(h\nu - E_g). \quad (3)$$

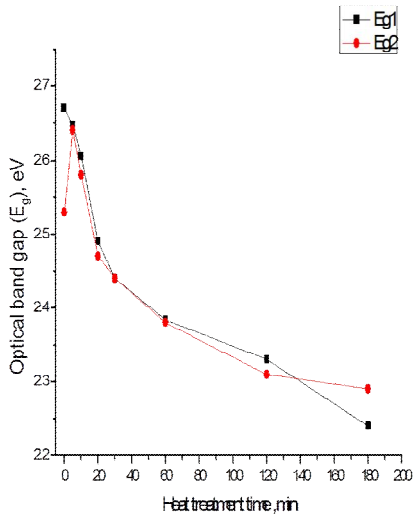

Fig. 2. Dependence of the bandgap vs. heat treatmenttime.

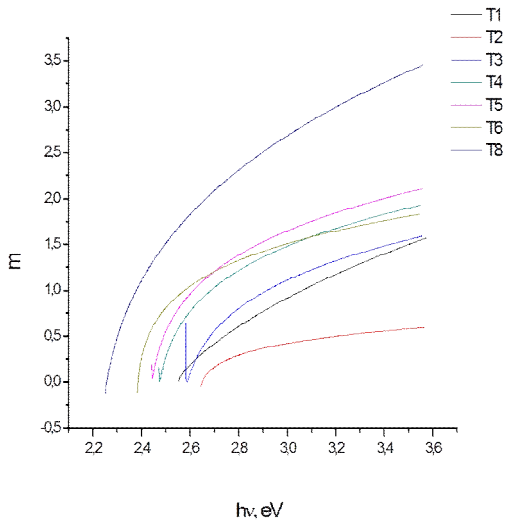

Fig. 3. The spectral dependence of the coefficient **m** in the strong absorption region.

The value of **m** was determined from the slope of $\ln(\alpha h\nu)$ *vs* $\ln(h\nu - E_g)$.

To determine the spectral dependence of the **m** was previously plotted $\ln(\alpha h\nu)$ vs. $\ln(h\nu - E_g)$. Dependence $\ln(\alpha h\nu)$ vs. $\ln(h\nu - E_g)$ was fitted to polynomial form. It was shown that this dependence is well described by a fourth-order polynomial. Further, the mathematical equation describing the dependence is derived by $\ln(h\nu - E_g)$. Figure 3 shows the spectral dependence of the coefficient m in the strong absorption region. As can be seen from the resulting dependency value m increases monotonically in the range (0 ÷ 3).This behavior m indicates that depending on the photon energy changes the nature of optical transition. If at the initial stage of formation of nanocrystals value of m is in the range of 0.5, which corresponds to the allowed direct transitions, further approaching to 3/2, which corresponds to the forbidden direct transitions. In order to get the law of change m vs. $h\nu$ the experimentally obtained dependence was approximating expression $m = K(h\nu - E_g)^c$.The experimental dependence is well described by this expression and the coefficient c for different samples varied within 0.36 ÷ 0.7.

3. Conclusions

Thus, by means of optical transmission spectra investigated the nature of optical transition in theCdS_xSe_{1-x} semiconductor nanocrystals, which are in different stages of formation. It is shown that the initial stage of formation of nanocrystals predominate the allowed direct transitions, further the forbidden direct transitions.

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DESIGN & MODELING OF INTEGRATED CIRCUITS

32/28 NM LOW POWER ORCA PROCESSOR WITH MULTI-VOLTAGE SUPPLY

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1. Introduction

The paper presents a method of power optimization, implemented on RISC architecture ORCA processor, aimed at reducing dynamic and static power consumption. Multi-voltage design method is one of the most effective power reduction methods, implemented by dividing circuit into separate power domains based on their power/performance requirements. Each domain then is supplied by separate power and ground rail.

2. ORCA Processor

ORCA is a 32-bit CPU microprocessor core. The sub-block CLOCK_GEN contains two PLLs (Phase Locked Loop) and a clock multiplier for the functional clocks [1]. Microprocessor has two main interfaces: PCI interface and source synchronous DDR interface for SDRAM. The processor core consists of a high-speed RISC machine with a power save mode. The BLENDER block is shut down during power save mode and RISC_CORE is slowed down to half its frequency (Fig.1).

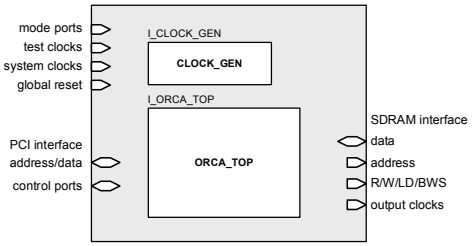


Fig. 1. ORCA

Except power saving ORCAhas two main modes - functional and test (Table 1.). In test mode, the clocks for functional mode are not used. All asynchronous interfaces between clock domains are isolated with dual-port FIFOs. The ORCA design contains six scan paths to enable high fault coverage for stuck-at fault testing on Automatic Test Equipment (ATE). These scan paths are essentially six long shift registers made up of all the multiplexed scan flip-flops in the ORCA design. The shift registers are enabled by device input pins test_mode and scan_en[2]. This design is intended to give an understanding of some issues that can occur during logic, full-chip, multi-clock designs. The seventh latch is used to avoid hold violations for clock gating circuitry in the BLENDER design (Fig. 2).

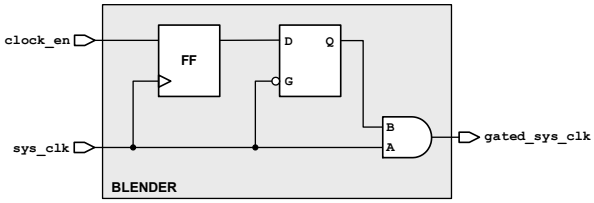


Fig. 2. Gated clock.

Table 1. ORCA processors modes

pm66en	Controls whether the PCI bus is operating at 33 (0) or 66 (1) MHz.
power_save	Controls whether RISC_COREoperates at 200 (0) or at 100 (1) MHz.
test_mode	Puts the chip in test-mode (1) or functional mode (0). Ensures that all flip-flops are clocked by either functional or test clocks. Also bypasses the clock disable in BLENDER, and selects the chip-level reset (prst_n) instead of the internally synchronized resets during test mode.

scan_en	Puts the registers in shift (1) or capture mode (0). During functional mode, registers are in capture mode. During test mode, this signal is toggled synchronously.

3. Design process

The design flow of ORCA is composed of traditional digital design flow with addition of power intent specification in Unified Power Format (UPF) [4]. This paper will describe all steps mentioned below and will present appropriate results. Design specification contains design logic and physical constraints along with description of dynamic and leakage power saving approach.

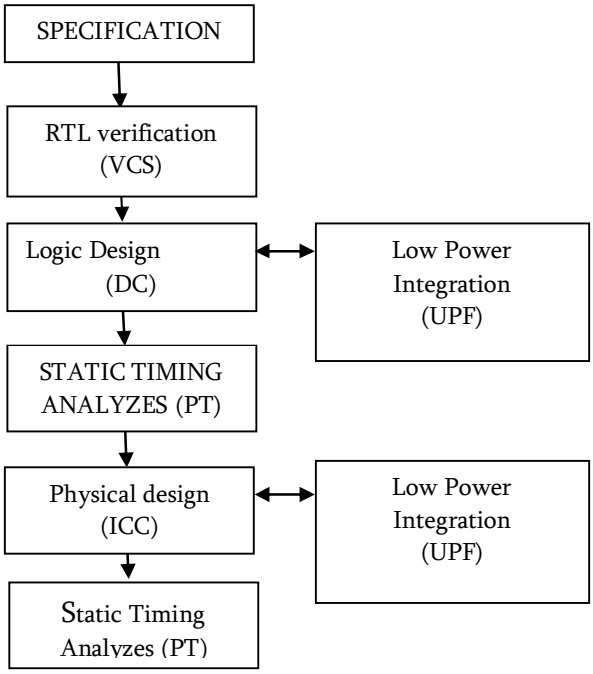
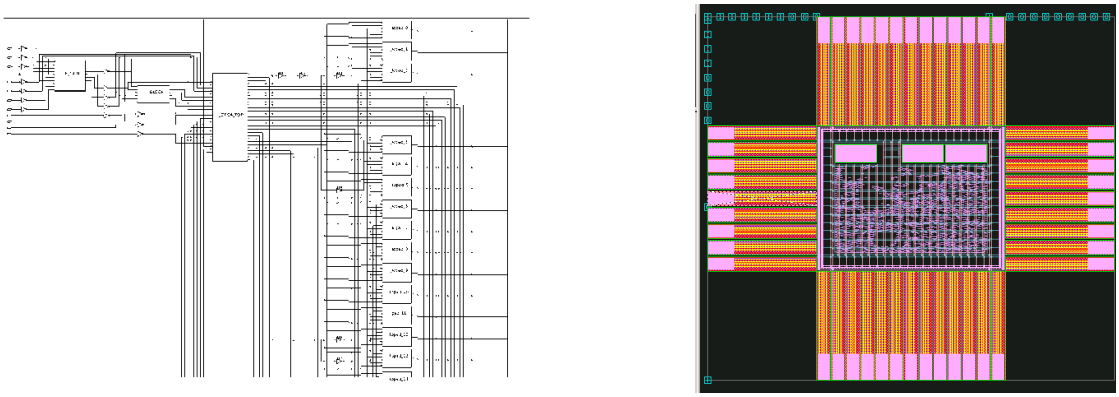


Fig. 3. Synopsys Digital Design Flow used.

Design was implemented with Synopsys digital design flow (Fig. 3). For the resulting circuit 60% (59.85%)of all power is spend on registers (Table 2.) and around 33% (32.92%) on combinational logic. Black boxes consume 6.79% and clock network: 0.33%.



a) logic circuit b) physical design

Fig. 4. Design of ORCA.

Table 2. Summarized results of reports timing/area/power

Frequency	200 Mhz
Data required time	20.21ns
Data arrrival time	-20.05 ns
Slack(MET)	0.15 ns
Total Power	88.52 mW
Macro/Black Box area	16340.796387 μm^2
Total cell area	589303.444805 μm^2
Total area	605644.241192 μm^2

4. Multi voltage implementation

Multi voltage design (Fig. 5) approach was used to reduce ORCA processor's power consumption [5].

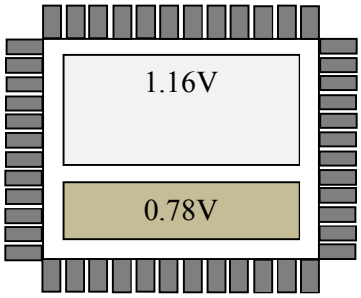


Fig. 5. Example of multi voltage method.

From the ORCA processor architecture RISC core was chosen as a low voltage domain operating at 0.78V while the rest is operating at 1.16V. Accordingly, a UPF description (Fig. 6) was developed which was used to provide power intent for digital design.

```
create_power_domain TOP -include_scope
create_power_domain RISC_CORE -elements I_ORCA_TOP/I_RISC_CORE -scope
I_ORCA_TOP/I_RISC_CORE
create_supply_port VDD -direction in
create_supply_net VDD
connect_supply_net VDD -ports VDD
create_supply_port VSS -direction in
create_supply_net VSS
connect_supply_net VSS -ports VSS
create_supply_port VDDRC -direction in
create_supply_net VDDRC
```

```
connect_supply_net VDDRC -ports VDDRC
create_supply_set SSET1 -function {power VDD} -function {ground VSS}
create_supply_set SSET2 -function {power VDDRC} -function {ground VSS}
set_domain_supply_net TOP -primary_power_net SSET1.power -primary_ground_net SSET1.ground
set_domain_supply_net I_ORCA_TOP/I_RISC_CORE/RISC_CORE -primary_power_net SSET2.power –
primary_ground_net SSET2.ground
add_port_state VDD -state {HV 1.16}
add_port_state VDDRC -state {LV 0.78}
add_port_state VSS -state {GND 0.000000}
```

Fig. 6. ORCA processor UPF description.

UPF diagram (Fig. 7) two power domains were defined: “RISC core” supplied by VDDRC with low voltage (LV 0.78) and rest of the processor supplied by regular-voltage VDD rail (HV 1.16). All required special cells (level shifters) were placed across the borders of the domains.

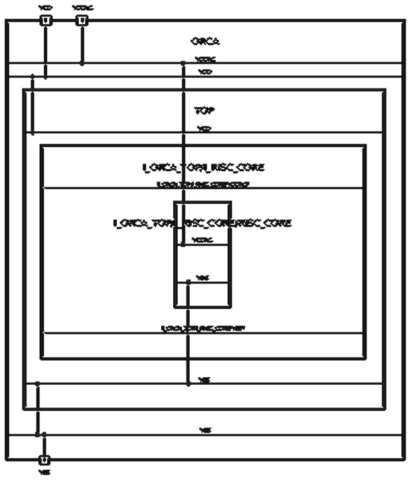


Fig. 7. ORCA processor multi voltage design UPF diagram.

UPF synthesis used same design constraints for frequency (for PCI clock at 75 MHz, System RISC clock at 200 MHz, SDRAM clock at 75 MHz) and physical utilization: 30% as standard synthesis. In the result, multi-voltage design with new values of timing/power/area was synthesized (Table 3).

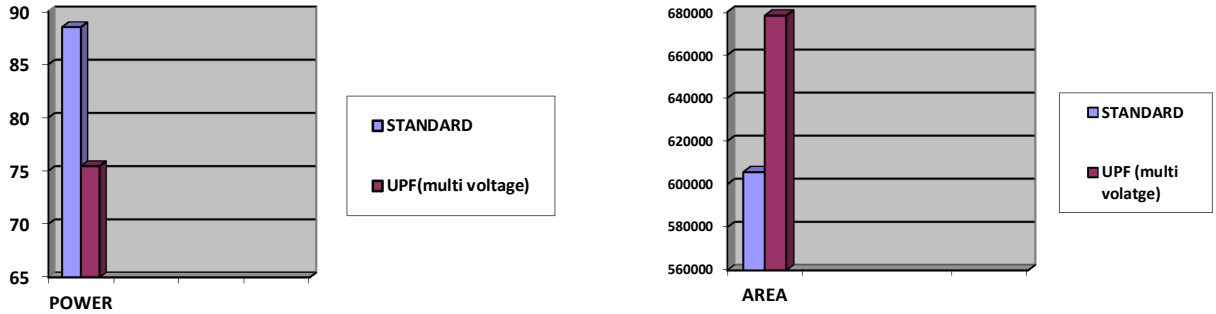
Table 3. timing/power/area

Frequency	200 Mhz
Data required time	20.21ns
Data arrrival time	-20.20 ns
Slack(MET)	0.01ns
Total Power	75.46 mW (-15%)
Macro/Black Box area	16340.796387 μm^2
Total cell area	661980.75374 μm^2 (+15%)
Total area	678321.550135 μm^2 (+12%)

Total power of the circuit was reduced by more than 15% compared to standard design (Fig. 8, a), at the same time total area of design increased by ~12% mainly in combinational cell are apart (15%) (Fig. 8, b).Timing changes are minor achieving required frequency of 200 MHz (with loss of 0.5 ns in input to output latency).

4. Conclusions

In the results multi voltage design approach proved efficient for decreasing power of ORCA processor (RISC core) with acceptable area loss. Future research will be aimed at implementing other low power techniques and fine-tuning power reduction to achieve more power efficiency with acceptable losses in area and timing.



a) b)

Fig. 8. Standard and UPF design comparison for a) power, b) area.

Acknowledgements

Design was implemented using SAED 32/28nm EDK [3] developed by Synopsys Armenia Educational Department. Synopsys tools Design compiler and IC Compiler provided by Synopsys Armenia Educational Department.

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IC DESIGN TECHNIQUES FOR PARAMETER UNCERTAINTY CONDITIONS

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1. Introduction

Continuous downscale of IC components leads to significant increase in technological deviations (TD), which occur during manufacturing process. This phenomenon brings an unpredictable deviation in physical, electrical and other parameters of IC elements, resulting low reliability and yield, as well as making both IC development and testing a complicated process. TDs are classified as accidental and non-accidental [2].

The sources of accidental TDs can be fluctuations in dopant concentration of transistor channel, as well as edge defects in transistor gates and interconnects. This kind of TDs can only be described by statistical functions. Non-accidental TDs have strictly periodic and predictable nature, which makes possible their prediction and modeling before the IC goes to manufacturing. However, as on initial state of IC development not sufficient information is known about the final layout of the design, these TDs are also modeled with the usage of statistical distribution functions [2].

IC timing characteristics are affected the most from the TDs. Primary factors which result a difference in timing parameters between design process and manufacturing are inaccuracies in circuit modeling and analysis, variations of environmental conditions, such as temperature, supply voltage etc. In order to design the IC while taking into account possible parameter deviations, a timing analysis is performed during development stage, which evaluates the influence of both accidental and non-accidental TDs [3]. There are two concepts for timing analysis, dynamic (DTA) and static (STA).

To implement DTA, a test environment must be designed in order to verify the timing characteristics and functionality of the circuit for defined input test signals. The efficiency of described method increases with the increase of the input test vectors. However, to implement DTA of acceptable precision on modern digital ICs, a great deal of machine recourses are required, which makes this method ineffective [4]. Currently only STA is performed for IC design.

2. Conventional Static Timing Analysis Methodology

Characterization of digital standard library cells with usage of conventional STA method is implemented with non-linear delay models. If the models contain timing information for different input signal slope and the output pole configurations, then, in order to implement probabilistic verification, additional models are needed with necessary information also about the dependency of timing characteristics from technological parameters. It is worth to mention that statistical delay model must be able to consider both internal and external deviations [5].

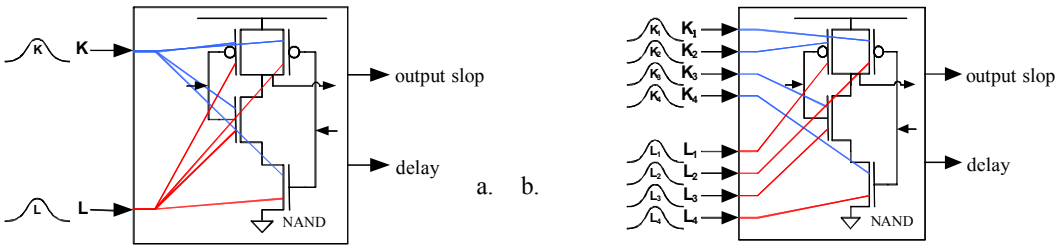


Fig. 1. The influence of internal (a) and external deviations on NAND block.

To precisely consider the external deviations (ED), the model must contain information about the effect of internal deviations (ID) as well, but unlike EDs (Fig. 1a), IDs have unique impact on each transistor of the test circuit (Fig. 1b). In this case, it is necessary to calculate the deviation of the circuit parameters for all transistors of the circuit. For timing model to encounter the above-mentioned information, extensive machine, human and time recourses are needed, which makes this modeling method practically inapplicable [6]. Considering the above-mentioned disadvantage of conventional STA modeling method, a new approach is proposed.

3. Proposed Static Timing Analysis Methodology

Proposed method for modeling the IDs, it is assumed that if every characteristic of each transistor varies according to Gaussian distribution independently from each other, then the output signal delay and slope of the circuit will also be distributed same way. The probability density of the Gaussian distribution is given by (1), where μ is the mean or expectation of the

distribution, while the σ parameter is the standard deviation.

$$f(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{(x-\mu)^2}{2\sigma^2}}, \quad (1)$$

$$X \sim N(\mu_x, \sigma^2{}_x), \quad (2)$$

$$Y \sim N(\mu_Y, \sigma^2{}_Y), \quad (3)$$

$$Z = X + Y, \quad (4)$$

$$Z \sim N(\mu_x + \mu_Y, \sigma^2{}_X + \sigma^2{}_Y). \quad (5)$$

It is known, that if the cell delay varies with Gaussian distribution, the signal delay of the whole chain can be modeled as a summary of Gaussian distributions, and will also distributed as in (2)-(5). For this configuration is suggested to perform Mote Carlo simulation to determine the output delay and signal slope values. Having the mean and +3σ, -3σ values of the distribution, they are assigned to a new variable, the +3σ, -3σ values of which will correspond the output signal distribution of the cell (Fig. 2). This approach enables to represent all IDs of the circuit with one variable, which provides sufficient efficiency to perform STA on digital ICs.

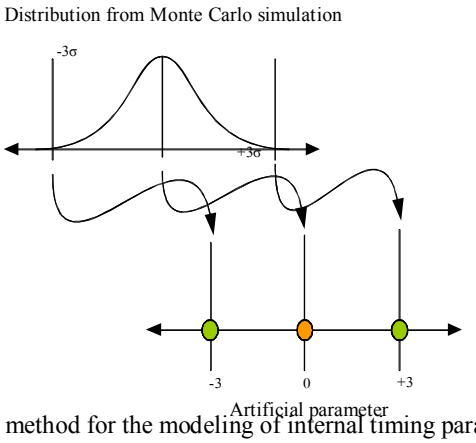


Fig. 2. Proposed method for the modeling of internal timing parameter deviations.

To test the proposed method a dual precision floating point circuit has been designed (Fig. 3). The design was implemented using three contemporary low power design techniques and performed STA for input to output delay chain with the proposed simulation method. For all designs a supply voltage of 0.95V was used, as well as same topology area restriction used equal to 150um^2. Simulations where performed for clock frequency equal to 500MHz. For all considered low power, design the statistical delay from req0 input pin to gnt0 output pin was calculated using both conventional and proposed STA techniques.

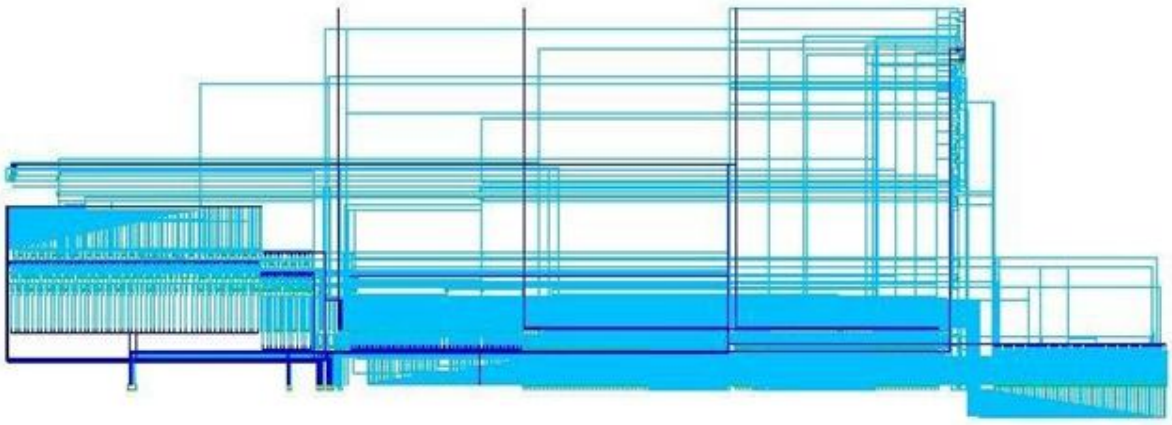
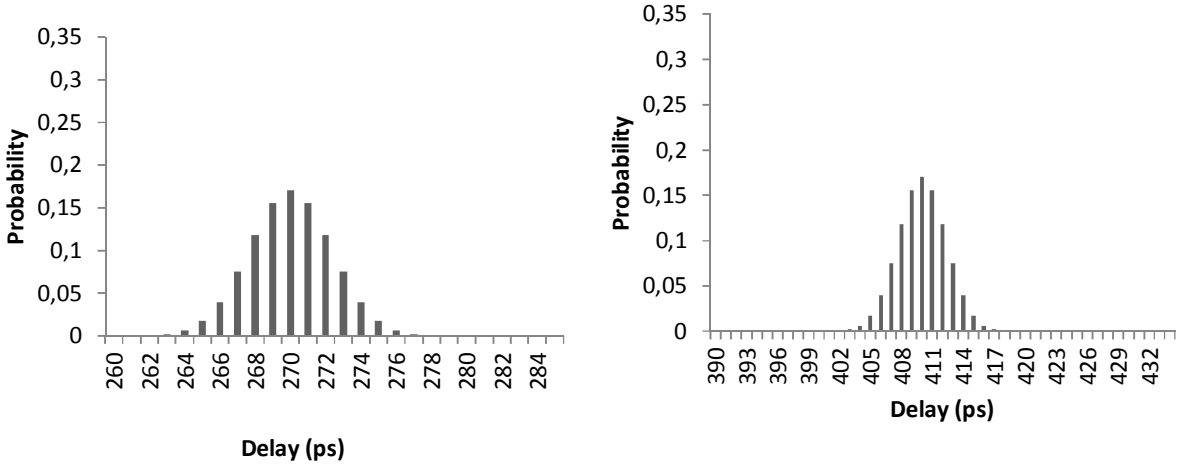


Fig. 3. Design of dual precision floating point circuit using supply voltage scaling technique.

4. Simulation results

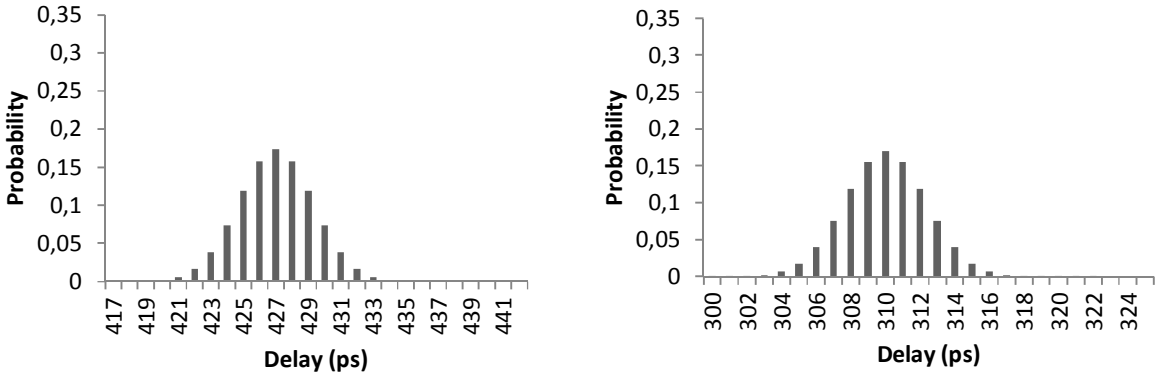
In order to verify the proposed STA method, statistical delay variations of input to output chain are measuring for different implementation of the proposed test design. As shown in Fig. 4 and Fig. 5, the average values for statistical delays for different low power technique vary from 270ps to 427ps.

For both proposed and conventional [7] STA methods CPU processing efficiency measurements were performed, which showed the superiority of the proposed technique in terms for processing duration from 7 to 9 times depending on the actual implemented low power design method.



a. b.

Fig. 4. Req0 to gnt0 statistical delay measurement for classic (a) and voltage scaling low power design techniques.



a. b.

Fig. 5. Req0 to gnt0 statistical delay measurement for multi-threshold (a) and clock gating (b) low power design techniques.

5. Conclusions

A novel method of static timing analysis was proposed to low power ICs and a respective testing circuit designed with the usage of three most common low power design techniques. For all designs, STA was performed to measure statistical delay for input to output chain. A statistical delay variation with average values from 270ps to 427ps was achieved for different low power design techniques. Compared to conventional STA method the proposed technique required 7-9 times less CPU processing duration, thus demonstrating the efficiency of proposed method.

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SELF-CALIBRATION METHOD FOR I/O TERMINATION RESISTANCE VARIATION ELIMINATION WITHOUT EXTERNAL REFERENCE RESISTOR

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1. Introduction

The inequality of output resistance and interconnect resistance will cause a signal reflection and therefore the information degradation in semiconductor circuits [1]. In purpose to avoid voltage reflections in transmissions lines of I/Os, various correction methods have been implemented to eliminate termination resistor and transmission line which are based on usage of an external resistor (Fig.1) [2]. Main disadvantage of these methods are the ineffective usage of IC area, as large area is required to locate the external resistor.

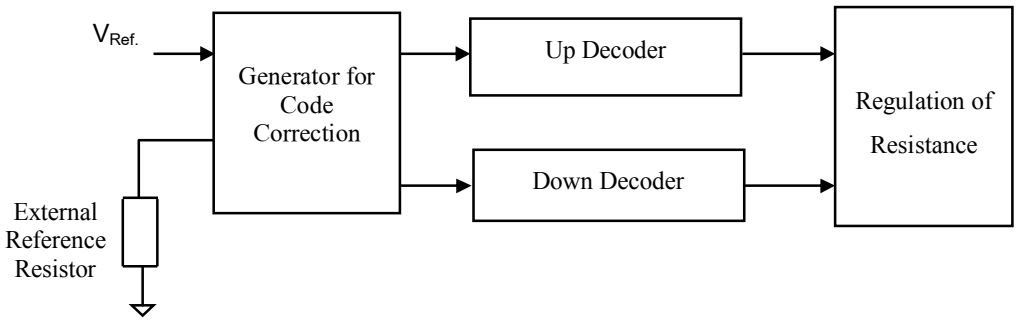

Fig. 1. Circuit for correction of transmitter resistor of I/Os based on external reference resistor.

A method of on-die resistance self-calibration for receiver and transmitter I/O devices, without external reference resistor is presented. The proposed calibration method detects the variation of the termination resistor and the transmission line and minimize it for all technology process, voltage and temperature (PVT) conditions. Resistance mismatch elimination method, using reference clock and dc current is provided [3]. A self-calibration technique for termination resistors mismatch elimination is implemented.

2. Proposed Self-Calibration Mechanism

The diagram representing self-calibration circuit principle is presented in Fig.2. The calibration starts with the "start" signal, during which the 'clk' signal should be present. "Control logic" is the control block, which triggers operation of the rest sub blocks with help of reference clock (synchro signal). The "Control Logic" block controls and regulates the delays of the clocks of the different blocks, providing the correct work between subblocks. Main functional blocks of the I/O edge resistance equalizer are the Integrator which based on the operational amplifier, the resistance chain (matrix) [4] and the analog to digital converter [5]. The other digital blocks provide the correct performance and stability of overall circuit, as well as the control functions and connection to subblocks.

At first the Control Logic block sends the "tclk" to the "Analog block" for integration, the another synchro signal to the ADC (Analog Digital converter) with binary encoded output, which gives binary codes to the Memory Resistors and after second integration also supports appropriate synchro signal to other block such as Memory registers, divider and to the "logic block" where are located memory devices, Successive Approximation Register (SAR), and other digital blocks which are synthesized by "Design Compiler" using of Verilog code [6]. At first due to controlling by Control logic block the SAR is reset to the initial state, by waiting the upcoming binary codes.

Getting adjusted binary codes, the "Control block" issues the "end" signal which informs that the calibration is completed and the output binary code is registered in the memory device.

3. Self-Calibration circuit operation principle

The integrator starts its work with positive slope of "tclk" which generates "Control block" when the "start" signal is active and after integration the output of the "Integrator and Resistance chain" (Fig. 2) will be defined as:

$$V_{out} = \frac{(V_{ref} - (Vdd - V_{ref}))\Delta t}{RC}. \quad (1)$$

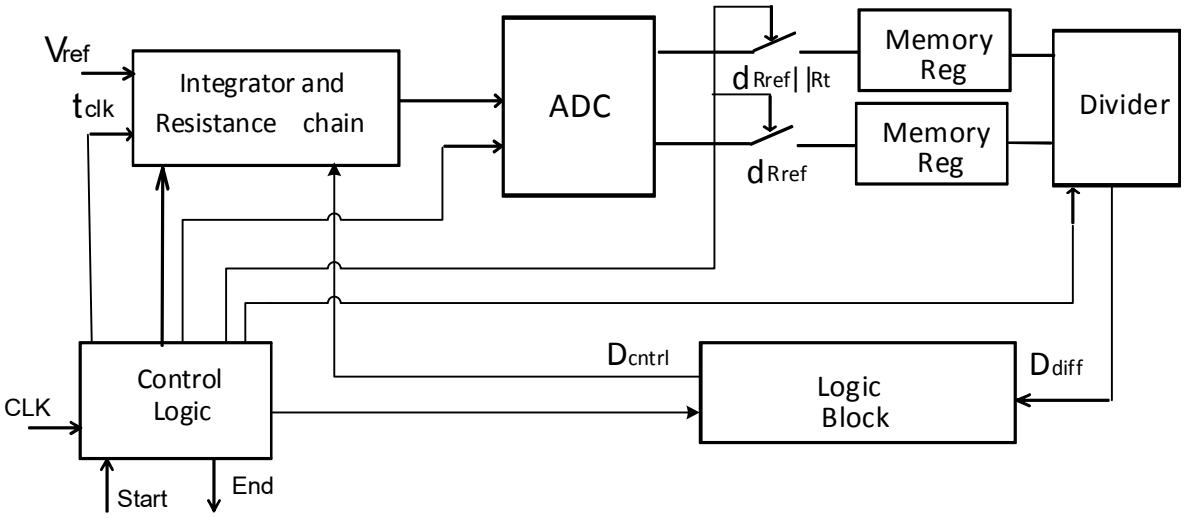

Fig. 2. Self-calibration circuit structure of I/O termination resistor variation.

The first integration begins when a bias voltage Vdd/2 is given to the one input of the operational amplifier, and the other is connected only to the constant resistance R=Rref without resistance chain. During the second integration, R resistance is used in parallel with the resistance chain of RT resistors R=Rref|| $\sum R_T$ where:

$$\sum R_T = \frac{R_b R_i \sum_{i=0}^{63} b_i}{R_b + R_i \sum_{i=0}^{63} b_i}. \tag{2}$$

Here Rb is the initial basic resistance with which must be connected the resistance chain, Ri is the unit resistor's value of the resistance chain (matrix) step and bi is the binary code.

The variations of the two integration voltages are adjusting the resistance value with help of OA's deep feedback loop. The comparison of the first and second integration voltages (Vout1, Vout2) is equivalent to 1 / R and 1 / (RT + R) comparison:

$$\frac{\Delta V_{out1}}{\Delta V_{out2}} = \frac{R_T}{(R_T + R_{ref})}. \tag{3}$$

Difference between V_{out} voltages will be caused only by resistors mismatch in the case, when both resistors (R and R|| R_T) are charged with the constant current[2].The corresponding ratio of two integrated voltages is appropriate the value of the resistance which will be corrected by the OA's deep feedback loop.

From the first integration's voltage where value ADC with binary encoded output gives the appropriate binary code dRref (Fig. 2) which is in this case is 6 bit which is saved in the first memory register. After getting the second code dRref||dRT, which appropriates voltage of the second integration voltage. Due to divider the difference code between two binary codes dRref and dRref||dRT is given to the logic block where it was compared with already exist ideal code, which was already counted by the Eq. (2) with the help of digital mechanism in "logic block" and the output Ddiff binary code, for which: Ddiff = F(dRideal,dRref/dRref||dRT). With the help of Decoder (6X64) Ddiff binary code is changed to the Dcntrl unitary code which from "Logic Block" goes to the "Analog block" to switch "on" or "off" the appropriate resisters of resistance chain. After getting the required code additional test cycle is performed by the control logic block in order to check the already generated binary code, which is the digitized value of the appropriate voltage, which corresponds to the corrected value of termination resistor and wire resistances. If the code is correct and the comparator does not switched, the "Control block" produces the "End" signal, which means that the operation is finished and the Dcntrl code is saved in memory register.

4. Simulation Results

Simulations have been performed using Hspice [7] simulator for a number of PVT corners including 5 main conditions TT, FF, SS, FS and SF processes with respective voltage and temperature values. Simulation results of the worst corners are presented in Table 1.

The results show that the proposed scheme correct resistors variation up to 8.6 % and as the conventional offset of resistors is more the corrected output offset is less. Increasing the number of the bits (d[n:0]) allows achieve higher output accuracy, which is limited by the sensitivity of comparator. The accuracy of the scheme is the deviation from the resistance value, depending on the scheme of parameters deviations such as non-ideality of comparator, which switches in case when the difference of input voltages is 0.086mV, which does not introduces no more than 10% total accuracy error. The maximum value resistance offset this technique is 8.6% (correspondent to the worst case of conditions), which is appropriate the standards of I/O devices as DDR2, DDR3, DDR4, LPDDR2, PCI and USB.

Table 1. Simulation results of worst corners for termination Resistors variation.

Resisrorsconvential offset	*Waited code*	*Getting code*	*Resistor proposed offset*
+25%	110111	110000	**7.4%**
-25%	011011	001111	**6.8%**
+15%	101100	100110	**7.8%**
-15%	001101	010011	**7.3%**
+10%	100110	101110	**8.6%**
-10%	010010	001011	**8.1%**

5. Conclusions

An on-die self-calibration method for receiver and transmitter I/O termination resistance is proposed and the respective circuit designed without external reference resistor. The presented solution of resistance mismatch elimination is based on usage of reference clock and dc current. It provides opportunity to measure the difference of the termination resistor and the transmission line impedance. The scheme of this method is the system of mixed signals. Circuit simulation is performed and the results of the simulation are presented.

The shown self-calibration technique can be used in the special input/output circuits of several standards such as Peripheral Component Interconnect (PCI), Universal Serial Bus (USB), Double Data Rate (DDR), etc.

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AN AVERAGED SMALL-SIGNAL MODEL OF THE BUCK CONVERTER IN DISCONTINUOUS CONDUCTION MODE

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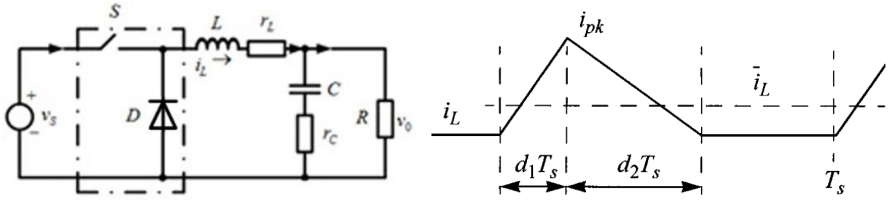
1. Introduction

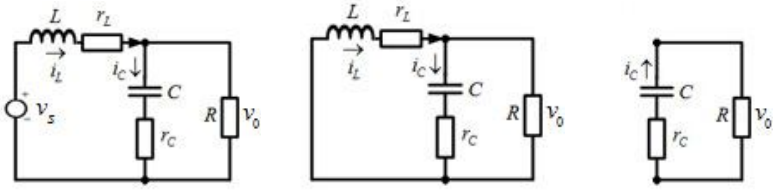
The PWM buck converters are widely used in various technical applications [1]. Such converters have two main working modes called, correspondingly, continuous and discontinuous conduction modes, which bring to essentially different dynamical characteristics of the converters [1-4]. The inductor current of the buck converter in the continuous conduction mode (CCM) is always positive, and in the discontinuous conduction mode (DCM), there exists an additional time interval in each switching cycle during which the inductor current is equal to zero. The various small-signal models of buck converters in the DCM are considered in [5-10] and many other papers and books. The derivation of the transfer functions of the buck converters in the CCM obtained by a time averaging of dynamic equations in state-space is presented in [11]. Below, an analogous derivation of transfer functions of the buck converters in the DCM is given and some new properties of the small-signal models are revealed.

2. The averaged model of the buck converter. As is known, dc-dc buck converters are nonlinear time-varying systems with periodic parameters. Therefore, the exact analytical investigation of their dynamics is an extremely complicated task. In practice, they usually resort to special approximate methods, which are based on the averaging of dynamics equations or on the so-called circuit averaging [1-8]. Below, in deriving the small-signal transfer functions of the buck converter in Fig. 1a in DCM, we will use, as in [11], the method of averaging the dynamics equations in state-space and subsequent linearization of averaged equations in the vicinity of the operating point. Note that in the adopted model of the buck converter in Fig. 1a, the parasitic resistance r_L of the inductor L and an additional ohmic resistance r_C connected in series with the capacitor C are allowed.



a) b)

Fig. 1.The adopted model of the buck converter (a) and the inductor current waveform in DCM (b).



a) $0 \le t < d_1T_S$ b) $d_1T_S \le t < (d_1+d_2)T_S$ c) $(d_1+d_2)T_S \le t < T_S$

Fig. 2. Equivalent subcircuits of the buck converter for different time intervals: a - the switch is turned on; b - the switch is turned off and $i_L(t) > 0$; c - the switch is turned off and $i_L(t) = 0$.

As mentioned above, in each cycling period T_S of the switch in the DCM, there is a time interval t during which the inductor current $i_L(t)$ reaches the zero value and preserves that value until the next closing of the switch. (Fig. 1b) [1-5]. Therefore, the circuit of the buck converter in Fig. 1a in this case can be represented by three equivalent subcircuits in Fig. 2, which correspond to three time intervals $0 \le t < d_1T_S$, $d_1T_S \le t < (d_1+d_2)T_S$ and $(d_1+d_2)T_S \le t < T_S$, where the designations d_1 and d_2 are clarified in Fig. 1b. The first of these intervals d_1T_S corresponds to the time during which the switch is turned on (i.e. $d_1 = D$, where D is the duty ration of the pulse-width modulated control signals), and the inductor current reaches at the end of that interval its peak value $i_{L\max}$. The second and the third intervals correspond to the time during which the switch is turned off, where the inductor current resets to zero at the end of the second interval. For each of the noted intervals it is possible to give, based on the equivalent subcircuits in Fig. 2, an exact dynamics description of the buck

converter. Let us choose as the state-space variables of the converter the inductor current $i_L(t)$ and the capacitor voltage $u_C(t)$. Then, introducing a two-dimensional state vector $x(t)$ with the components $x_1(t) = i_L(t)$ and $x_2(t) = u_C(t)$, we can put down for the subcircuit in Fig. 2a (i.e. for the interval $0 \le t < d_1 T_S$) the following equations

$$\begin{aligned}
&\frac{dx_1(t)}{dt} + \left[\frac{Rr_L + Rr_C + r_L r_C}{L(R + r_C)}\right] x_1(t) + \frac{R}{L(R + r_C)} x_2(t) = \frac{1}{L} v_S(t), \\
&\frac{dx_2(t)}{dt} = \frac{R}{C(R + r_C)} x_1(t) - \frac{1}{C(R + r_C)} x_2(t), \\
&v_0(t) = \frac{Rr_C}{R + r_C} x_1(t) + \frac{R}{R + r_C} x_2(t),
\end{aligned} \tag{1}$$

or, in the vector- matrix form,

$$\begin{aligned}
&\frac{dx(t)}{dt} = A_1 x(t) + b_1 v_S(t), \\
&v_0(t) = c_1 x(t),
\end{aligned} \tag{2}$$

where

$$A_1 = \begin{bmatrix} -\dfrac{Rr_L + Rr_C + r_L r_C}{L(R + r_C)} & -\dfrac{R}{L(R + r_C)} \\ \dfrac{R}{C(R + r_C)} & -\dfrac{1}{C(R + r_C)} \end{bmatrix}, \quad b_1 = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix}, \quad c_1 = \begin{bmatrix} \dfrac{Rr_C}{R + r_C} & \dfrac{R}{R + r_C} \end{bmatrix}, \tag{3}$$

and the input function $v_S(t)$ represents, as in [1], the fact that the input voltage V_S can be time-varying function.
The corresponding vector equations for the second interval $d_1 T_S \le t < (d_1 + d_2) T_S$, during which the switch is turned off and the inductor current is not zero, have an analogous form

$$\begin{aligned}
&\frac{dx(t)}{dt} = A_2 x(t) + b_2 v_S(t), \\
&v_0(t) = c_2 x(t).
\end{aligned} \tag{4}$$

Since the subcircuit with an open (turned off) switch in Fig. 2b differs from the subcircuit in Fig. 2a only by the value $v_S(t) = 0$, it can be shown that the matrix A_2 and vectors b_2 an c_2 in (4) are given by the expressions

$$A_2 = A_1, \quad b_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}, \quad c_2 = c_1. \tag{5}$$

Finally, for the third time interval $(d_1 + d_2) T_S \le t < T_S$ with zero inductor current we have, on the base of the subcircuit in Fig. 2c, the following equations

$$\begin{aligned}
&\frac{dx(t)}{dt} = A_3 x(t) + b_3 v_S(t), \\
&v_0(t) = c_3 x(t),
\end{aligned} \tag{6}$$

where, allowing for $i_L(t) = const = 0$, we get

$$A_3 = \begin{bmatrix} 0 & 0 \\ 0 & -\dfrac{1}{C(R + r_C)} \end{bmatrix}, \quad b_3 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}, \quad c_3 = \begin{bmatrix} 0 & \dfrac{R}{R + r_C} \end{bmatrix}. \tag{7}$$

Note that if the coefficient d_1 in Fig. 1b is determined only by the duty ratio D, that is $d_1 = D$, the coefficient d_2 depends on the parameters of the buck converter, switching period T_S and input voltage $v_S(t)$. In deriving the averaged model of the buck converter in DCM, the algebraic dependence of d_2 on D and on the parameters of the converter should be derived. That will allow to exclude d_2 from dynamics equations and to obtain a model expressed only through the averaged values of the state variables.

Using the standard approach based on neglecting of the output voltage ripple [1, 3], it can be shown that

$$d_2 = \frac{1}{2}\left(-D + \sqrt{D^2 + 4K}\right), \text{ where } K = 2L / \left(R + r_L\right) T_S. \tag{8}$$

Let us introduce an important for the following analysis value D_{pos}, which is the relative duration of positive pulses of the inductor i_L and which, taking into account (8), is equal to

$$D_{pos} = d_1 + d_2 = D + d_2 = \frac{1}{2}\left(D + \sqrt{D^2 + 4K}\right). \tag{9}$$

That value is always less than one and, evidently, is equal to one on the border of continuous and discontinuous conduction modes. Allowing for (8) and (9) it can be shown that the formula for the gain D_{DM} of the buck converter in Fig. 1a with respect to the input voltage is

$$D_{DM} = \frac{V_0}{V_S} = \frac{RD}{\left(R + r_L\right) D_{pos}}. \tag{10}$$

Thus, as opposed to the CCM, where the gain D_{DM} is equal to the duty ratio D [1-4], the gain D_{DM} (10) depends nonlinearly on D, inductance L, load resistance R, parasitic resistance r_L and switching (cycling) period T_S. Besides, the gain D_{DM} for $D_{pos} < 1$ is always greater than the corresponding gain D in CCM.

Application of the well-known averaging technique to the state-space differential equations (1)-(7) yields

$$\begin{aligned} \frac{dx(t)}{dt} &= \left[\left[d_1(t) + d_2(t)\right] A_1 + \left[1 - d_1(t) - d_2(t)\right] A_3\right] x(t) + d_1(t) b_1 v_S(t), \\ v_0(t) &= \left[d_1(t) + d_2(t)\right] c_1 x(t) + \left[1 - d_1(t) - d_2(t)\right] c_3 x(t), \end{aligned} \tag{11}$$

where generally it is assumed that the coefficients d_1 and d_2 are functions of time [1,5], and, for simplicity, the adopted in equations (1)-(7) designations for the time-averaged vector $x(t)$ and variable $v_S(t)$ are preserved.

Allowing for (1)-(7), we get instead of (11) the following modified averaged model of the buck converter in DCM, where for brevity of the notation the dependence on t is omitted,

$$\frac{d}{dt}\begin{bmatrix} i_L \\ u_C \end{bmatrix} = \underbrace{\begin{bmatrix} -\dfrac{Rr_L + Rr_C + r_L r_C}{2L(R + r_C)}\left(d_1 + d_2\right) & -\dfrac{R}{2L(R + r_C)}\left(d_1 + d_2\right) \\ \dfrac{R}{2C(R + r_C)}\left(d_1 + d_2\right) & -\dfrac{1}{C(R + r_C)} \end{bmatrix}}_{A_\Sigma} \begin{bmatrix} i_L \\ u_C \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} d_1 v_S, \tag{12}$$

or, in the matrix form

$$\frac{dx(t)}{dt} = A_\Sigma x(t) + d_1(t) b_1 v_S(t). \tag{13}$$

The expression for the output voltage has the form

$$v_0(t) = \frac{R}{R + r_C}\left[\left(d_1(t) + d_2(t)\right) r_C,\ 1\right] x(t) = \frac{R}{R + r_C}\left[\left(d_1(t) + d_2(t)\right) r_C i_L(t) + u_C(t)\right]. \tag{14}$$

As can be seen from (13)-(14), the dynamics investigation of the buck converter in DCM is considerably more difficult task than the same task for CCM, since for the given duty ratio $D = d_1$, the matrix A_Σ in (13) depends on the coefficient d_2 (8), which depends in a nonlinear manner on D and on the parameters of the converter (recall, that in CCM the matrix A and vector c_0 are constant [1,11]).

2. *Transfer functions of the buck converter*

The derivation of transfer functions of the buck converter requires linearization of the dynamics equations of the nonlinear averaged model in the vicinity of some operating point. Let us exploit for that purpose the classical procedure of linearization of nonlinear differential equations [12]. In general form, the latter can be written as

$$\begin{aligned} \frac{dx(t)}{dt} &= f(x(t), u(t)), \\ y(t) &= g(x(t), u(t)). \end{aligned} \tag{15}$$

In our case, the two-dimensional state vector $x(t)$ has the components $x_1(t) = i_L(t)$ and $x_2(t) = u_C(t)$, the scalar output $y(t)$ is equal to $v_0(t)$ in (14), the two-dimensional input vector $u(t)$ has the components $u_1(t) = v_S(t)$ and $u_2(t) = d_1(t)$, and the functions $f(x(t), u(t))$ and $g(x(t), u(t))$, on the basis of (12) and (14), are equal to

$$f(x,u)=\begin{bmatrix} -\dfrac{Rr_L+Rr_C+r_Lr_C}{2L(R+r_C)}\left(u_2+\sqrt{u_2^2+4K}\right)x_1- \\ \qquad -\dfrac{R}{2L(R+r_C)}\left(u_2+\sqrt{u_2^2+4K}\right)x_2+\dfrac{1}{L}u_1u_2 \\ \dfrac{R}{2C(R+r_C)}\left(u_2+\sqrt{u_2^2+4K}\right)x_1-\dfrac{1}{C(R+r_C)}x_2 \end{bmatrix},$$

$$g(x,u)=\frac{R}{R+r_C}\left[\frac{1}{2}\left(u_2+\sqrt{u_2^2+4K}\right)r_Cx_1+x_2\right], \tag{16}$$

where for brevity the dependence of vectors $x(t)$ and $u(t)$ on time t is omitted.

Let us represent all the averaged time-varying functions in (15) in form

$$x(t)=X+\tilde{x}(t),\quad v_0(t)=V_0+\tilde{v}_0(t),\quad u(t)=U+\tilde{u}(t),\ \textbf{где}\ u_1(t)=V_S+\tilde{v}_S(t),\quad u_2(t)=D+\tilde{d}(t),$$

where all the deviations $\tilde{x}(t),\tilde{v}_0(t),\tilde{v}_S(t),\tilde{d}(t)$ are assumed small, and X, V_0, V_S and D are constant that correspond to the operating point. Then, assuming that the operating point is an equilibrium point, that is

$$f(x(t),u(t))\Big|_{\substack{x(t)=X\\u(t)=U}}=0,$$

the corresponding (constant) output signal is equal to

$$V_0=g(x(t),u(t))\Big|_{\substack{x(t)=X\\u(t)=U}}.$$

The procedure of linearization of equations (15) consists in expansion, assuming the deviations from the operating points small, of nonlinear functions $f(x(t),u(t))$ and $g(x(t),u(t))$ in the Taylor series and subsequent neglecting all the terms besides the linear one. As a result, the equations (15) are replaced by the following linear equations

$$\begin{aligned} \frac{d\tilde{x}(t)}{dt}&=A\tilde{x}(t)+B\tilde{u}(t),\\ \tilde{v}_0(t)&=C\tilde{x}(t)+E\tilde{u}(t), \end{aligned} \tag{17}$$

where the matrices A, B and the row vectors C and E are given by the expressions

$$A=\left[\frac{\partial f(x,u)}{\partial x}\right]\Bigg|_{\substack{x=X\\u=U}},\quad B=\left[\frac{\partial f(x,u)}{\partial u}\right]\Bigg|_{\substack{x=X\\u=U}},\quad C=\left[\frac{\partial g(x,u)}{\partial x}\right]\Bigg|_{\substack{x=X\\u=U}},\quad E=\left[\frac{\partial g(x,u)}{\partial u}\right]\Bigg|_{\substack{x=X\\u=U}}. \tag{18}$$

Allowing for (9), (18) and the form of functions $f(x(t),u(t))$ and $g(x(t),u(t))$ in (16), the elements of the matrices A, B and the row vectors C and E in (18) are equal to

$$A=\begin{bmatrix} -\dfrac{(Rr_L+Rr_C+r_Lr_C)D_{pos}}{L(R+r_C)} & -\dfrac{RD_{pos}}{L(R+r_C)} \\ \dfrac{RD_{pos}}{C(R+r_C)} & -\dfrac{1}{C(R+r_C)} \end{bmatrix},$$

$$B=\begin{bmatrix} \dfrac{1}{L}D & \dfrac{1}{L}V_S-\dfrac{RD_{pos}}{L(R+r_C)\sqrt{D^2+4K}}X_2 \\ 0 & 0 \end{bmatrix},$$

$$C=\frac{R}{R+r_C}\left[r_CD_{pos},\ 1\right],\quad E=\frac{R}{R+r_C}\left[0,\ \frac{r_CD_{pos}}{\sqrt{D^2+4K}}X_1\right].$$

Note that the linearized equations (17) actually connect the scalar output $\tilde{v}_0(t)$ with two input variables $\tilde{d}(t)$ and $\tilde{v}_S(t)$. Therefore, in accordance with the principle of superposition [12], the impact of these variables on the output of the buck converter can be analyzed independently.

Following the common technique of deriving transfer functions of linear systems from the state-space equations, one should perform the Laplace transform of the equations (17) with zero initial conditions, and exclude from the obtained algebraic equations the vector $x(s)$, where s is the Laplace variable [12]. This yields the following complex equation with respect to scalar output variable $\tilde{v}_0(s)$:

$$\tilde{v}_0(s)=W(s)\tilde{u}(s),$$

where the transfer function $W(s)$ of size 1×2 has the form

$$W(s)=\left[W_V(s),W_D(s)\right]=C(sI-A)^{-1}B+E\,. \tag{19}$$

The scalar transfer functions $W_V(s)$ and $W_D(s)$ in (19) connect $\tilde{v}_0(s)$ with the input variables $\tilde{u}_1(s)=\tilde{v}_S(s)$ and $\tilde{u}_2(s)=\tilde{d}(s)$. The expressions for $W_V(s)$ and $W_D(s)$, derived on the base of (19), have the form

$$W_V(s)=\frac{D_{pos}RD\left\{r_C\left[s+\dfrac{1}{C(R+r_C)}\right]+\dfrac{R}{C(R+r_C)}\right\}}{L\left(R+r_C\right)\Delta(s)}\,, \tag{20}$$

$$W_D(s)=\frac{RV_S}{G\sqrt{D^2+4K}}\left\{\frac{M_0s+M_1}{LC\left(R+r_C\right)\Delta(s)}+r_CD\right\}\,, \tag{21}$$

where

$$G=\left[Rr_L+Rr_C+r_Lr_C+R^2D_{pos}\right],\;\; M_0=r_C2KCG+RLD,$$

$$M_1=2KG+\frac{D_{pos}R}{(R+r_C)}\left[Rr_L+Rr_C+r_Lr-r_CD_{pos}RD\right],$$

and the characteristic equation $\Delta(s)=\det(sI-A)$ is equal to

$$\Delta(s)=s^2+\frac{\left[C(Rr_L+Rr_C+r_Lr_C)D_{pos}+L\right]}{LC(R+r_C)}s+\frac{GD_{pos}}{LC(R+r_C)^2}\,.$$

It should be noted that the transfer functions $W_V(s)$ and $W_D(s)$ have, correspondingly, left-half plane zeros at $Z_V=-1/r_CC,\; Z_D=-M_1/M_0.$ Besides, the transfer function $W_D(s)$ contains an algebraic term, which immediately transfers the input signal to the output with the gain r_CD. For an ideal buck converter, that is for $r_L=r_C=0$, the transfer functions $W_V(s)$ (20) and $W_D(s)$ (21) take on considerably simpler form:

$$W_V(s)=\frac{D_{pos}}{LC\left(s^2+\dfrac{1}{CR}s+\dfrac{1}{LC}D_{pos}^2\right)}D\,,\qquad W_D(s)=\frac{V_S\left[(LD)s+2KRD_{pos}\right]}{LCRD_{pos}\left(\sqrt{D^2+4K}\right)\left(s^2+\dfrac{1}{CR}s+\dfrac{1}{LC}D_{pos}^2\right)}\,. \tag{22}$$

The transfer function $W_v(s)$ in this case has no zeros, and $W_D(s)$ does not contain the algebraic term and has a zero at the point

$$Z_D=-\frac{2KR}{LD}D_{pos}=-\frac{2}{DT_S}\left(D+\sqrt{D^2+\frac{8L}{RT_S}}\right).$$

For $s=0$, instead of (22) we get well-known expressions [1]

$$W_V(0)=\frac{2D}{D+\sqrt{D^2+4K}}\,,\qquad W_D(0)=\frac{8KV_S}{\left(\sqrt{D^2+4K}\right)\left(D+\sqrt{D^2+4K}\right)^2}\,.$$

Example. Let us consider a buck converter with the following parameters: $D=0.1,\; f_S=100\;kHz\,,\; r_C=0.05\;\Omega,$ $L=3.3\;\mu H, r_L=80\;m\Omega,\;\; C=75.2\;\mu F, R=1.0\;\Omega, V_S=12\;V.$ It can be shown that the buck converter with such parameters values is in DCM. The transfer function $W_D(s)$ (21) is equal to

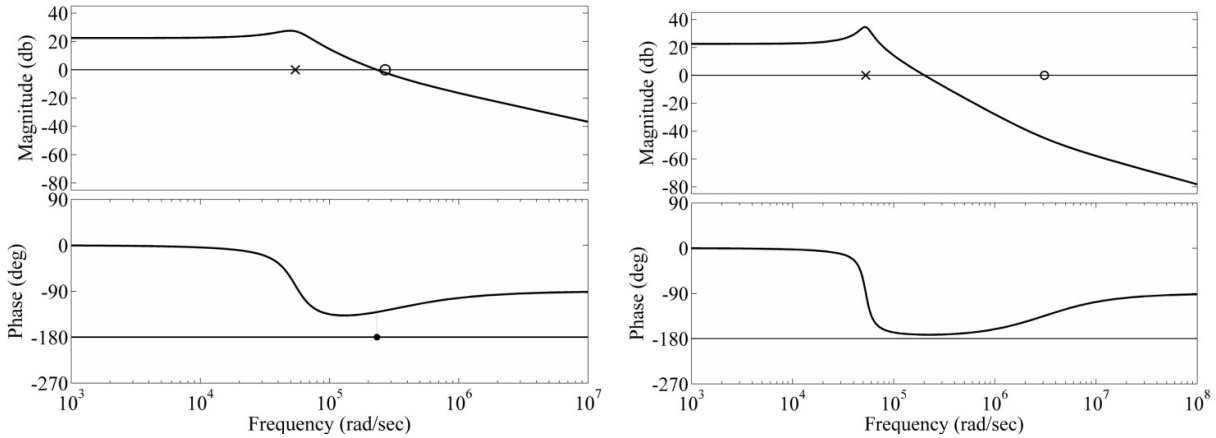
$$W_D(s)=\frac{145117.66\left(s+269156.4\right)}{s^2+32000.86s+2946351308.4}+0.039591 \tag{23}$$

and has two complex-conjugate poles $\mathrm{p}_{1,2}=-16000.43\;\pm j51868.46$ and one zero $Z_D=-269156.4$. In the case of ideal converter, that is for $r_L=r_C=0$, the transfer function $W_D(s)$ (23) has the form

$$W_D(s)=\frac{12222.7\left(s+\;3086419.75\right)}{s^2+13297.87s+2798373809}\,, \tag{24}$$

i.e. the algebraic term in this case disappears The poles and zero of that transfer function are $\mathrm{p}_{1,2}=-\,6648.93\;\pm j52480.1$, $Z_D=-3086419.75$. The Bode diagrams of the transfer functions $W_D(s)$ (23) and (24) are shown in Fig. 4.

As can be seen from the Bode diagrams in Fig. 4, the presence of nonzero resistance $r_C = 0.05\ \Omega$ increases the phase margin of the transfer function $W_D(s)$, which improves the small-signal transient responses of the buck converter in DCM.



a) $r_L = 0$, $r_C = 0.05\ \Omega$ b) $r_L = r_C = 0$

Fig. 4. Bode diagrams of the transfer function $W_D(s)$.

3. Conclusions

The issues of derivation of transfer functions of the buck converter in the discontinuous conduction mode by a time-averaging the dynamics equations of the converter in the state-space and subsequent linearization in the vicinity of the operating point are discussed. It is shown, that, as opposed to the case of continuous conduction mode, the transfer function of the ideal converter with respect to the duty ratio D has a left-half plane zero. Another difference is that in case of ohmic resistance in series with the capacitor both transfer functions with respect to the input voltage and D have different zeros and, besides, the transfer function with respect to D contains an algebraic term.

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DATA GENERATOR AND SYNTHESIZABLE MONITOR FOR USB3.0 LINK LAYER TESTING

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1. Introduction

Functional verification (FV) is an important step in development of today's complex designs. FV is widely recognized as a most time and resource consuming part of the design development. In fact, it theoretically rises exponentially with hardware complexity doubling exponentially with time [2]. Figure 1 shows the statistics of the SOC designs in terms of design complexity (logic gates), design time (engineer years), and verification complexity (simulation vectors) [3].

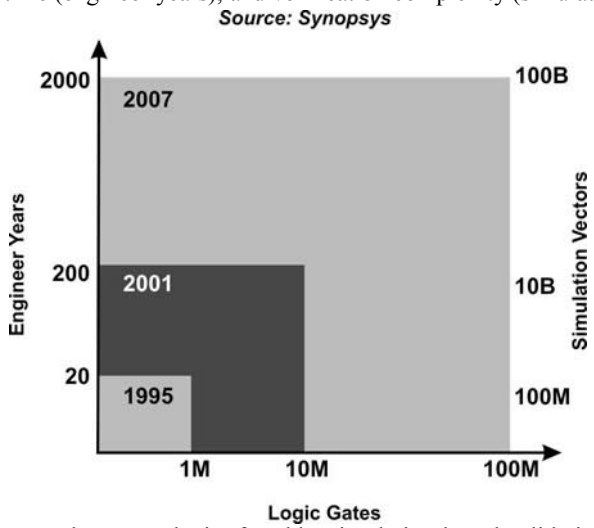

Fig. 1. Thestudy highlights the tremendous complexity faced by simulation-based validation of complex SOCs. A complex SOC will need 2000 engineer years to write 25 million lines of register-transfer level (RTL) code and one trillion simulation vectors for functional verification.

The author of [1] identifies four major challenges of verification as: dealing with enormous state space size, detecting incorrect behavior, lack of golden reference model and lack of a comprehensive functional coverage matric.

The scale of the state space is the first verification challenge. To verify exhaustively that a chip is functionally correct, the verification engineer needs to check that each possible current state and each possible input combination yields the correct next state. This challenge is observable during USB development. Only link state machine of USB3.0 has 12states and each of them is intended for some specific task [4]. For example U1,U2, U3 are used for power saving, Recovery as it name suggests to handle different error situations and transitional state from power saving states to U0 (operational state, where actual data transfer happens), Rx.Detect and Polling to establish initial connection and etc. Each of these states i.e. functionalities shall be verified. Verification of the full controller which includes buffer management units, control and status registers, application interface controllers (AHB, AXI etc.), power management units and units for protocol support is a complex task.The second verification challenge is detecting when the design violates the expected behavior or specification. A lot of transitions are possible and the verification engineer must identify whether or not the design acted correctly based on the current state and input. Third and fourth respectively the lack of a golden reference model and the lack for a comprehensive functional coverage metric are the most important reasons of bugs in the design. There are several articles which propose approaches to resolve verification problems described above. Prototyping is an effective tool and can be used to solve the first issue. In [8] software-hardware co-emulation environment is presented. The main drawbacks of this approach are the limitations connected with performance of the verificationenvironment. FPGA prototype designs using Synthesizable SystemVerilog Assertions (SSVA) as a solution to second challenge are proposed in [5] and [6]. Open Control Protocol (OCP) monitor is taken as an example implementationin [5].There are many articles which provide methodologies to address fourth challenge during simulation. Solution for fourth challenge by prototyping is introduced in [7]. In this article we'll try to address these challenges. The first issue is solved by braking USB design into smaller parts and using the high speed of verification which is provided by prototyping.We overcame the second and the fourth challenges by exploiting synthesizable assertion placed in monitors and within device under test. The third issue is partially solved by

implementing driver and monitor to emulate upper layers of USB and check the protocol. Verification of USB3.0 link layer is used as an example.

2. Verification Environment Architecture

The verification environment is presented in Fig. 2Two Synopsys HAPS51T boards are used as a platform for our prototyping environment. There are no PCs in environment and it's a full hardware solution. The added hardware is not limiting the performance as it supports onlynecessary commands and it doesn't interpret the received data. Every component is describedin following sections.

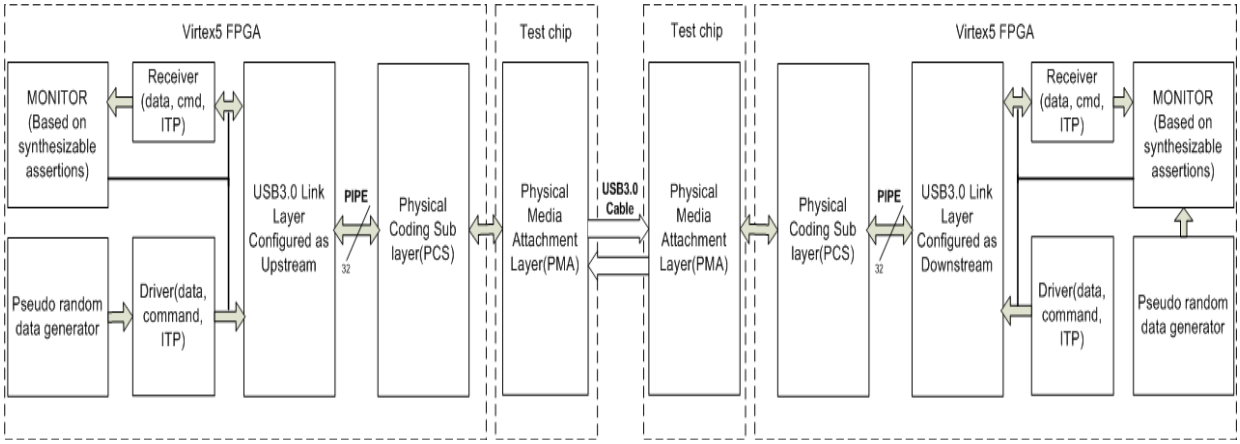

Fig. 2. Proposed USB3.0 Link Layer Verification environment.

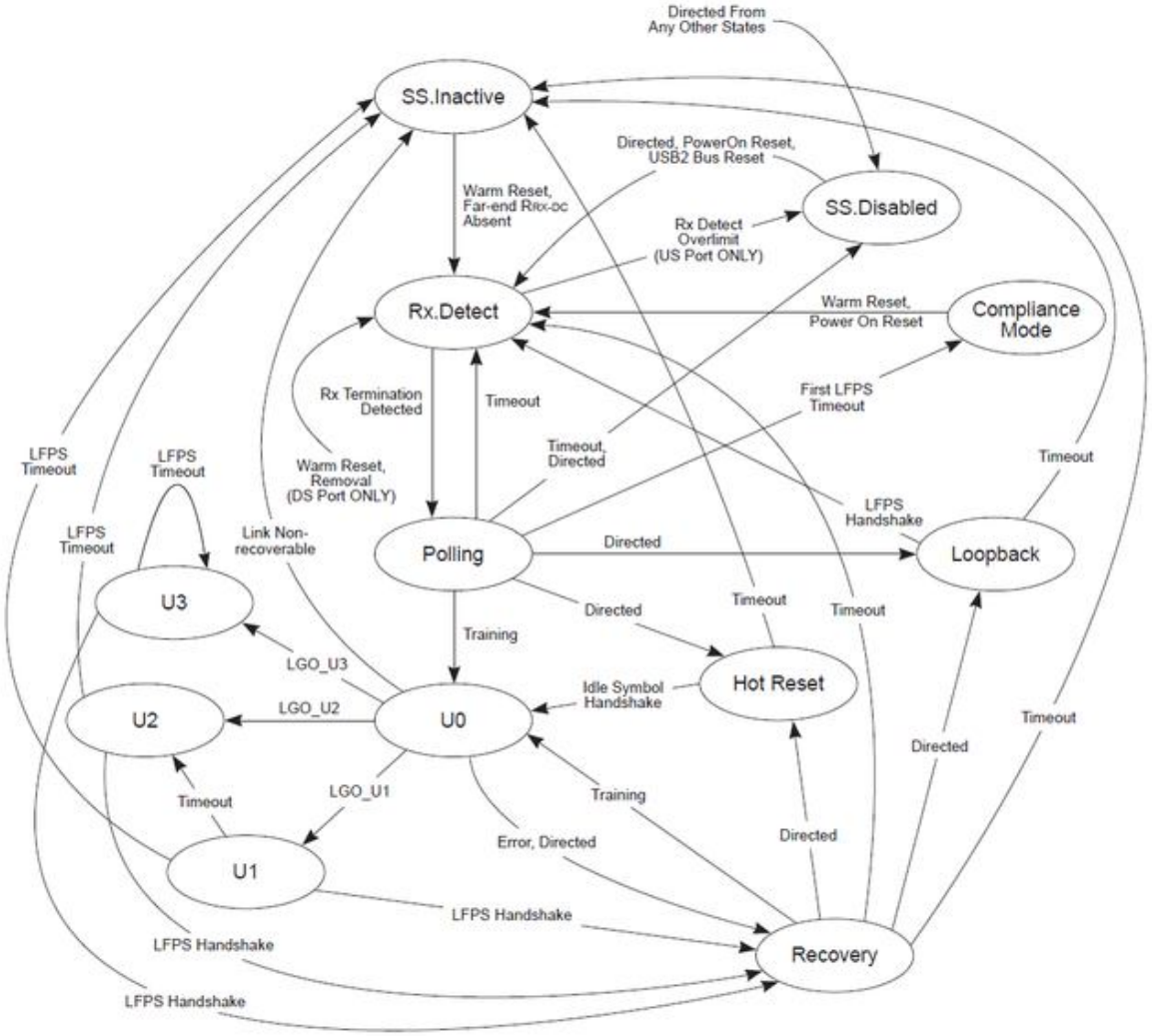

Fig. 3. Link layer FSM. Source: USB3.0 specification.

3. USB3.0 Link Layer

Usually the same USB3.0 link layer RTL is used in all types of USB3.0 designs(host, hub and device controllers) so developing and testing it should be performed properly. According to [4] link layer is intended to establish initial connection, construct packets based on data from upper layers and support low power mode entry requests and send a request if required. One of the things which make link layer development hard is its duty to interoperate with different physical interfaces.

The design consists of Tx/Rx data paths and a global finite state machine (FSM) which isused to control USB connections. Data paths are transmitting/receiving data, link commands and Isochronous Timestamp Packets (ITP), each of them has its own control FSM.The link layer also facilitates link training, link testing/debugging, and link power management. This is accomplished byLink Training Status State Machine (LTSSM).The LTSSM and all possible transitions between states are presented in Fig. 3.

4. USB physical layer

Thephysical layer handles the low level USB SuperSpeed protocol and signaling. In our environment it is divided into two parts: Physical Coding Sub layer and Physical Media Attachment layer. The combination of these parts forms transceiver and receiver. The receiver is presented in Fig. 4.

PSC is pure digital and therefore it is implemented it on FPGA. PCS contains: 8b/10b encoder/decoder, elastic buffer and descrambler/scrambler. PMA contains analog parts. Receiver PMA does the following: differential receiver detection, equalization, clock recovery, data recovery and serial to parallel conversion. It is possible to use Gigabit transceivers/receivers to implement this part but in this work Synopsys test chip is used. The full description of above mentions feature and transceiver is in Chapter 6 of [4].

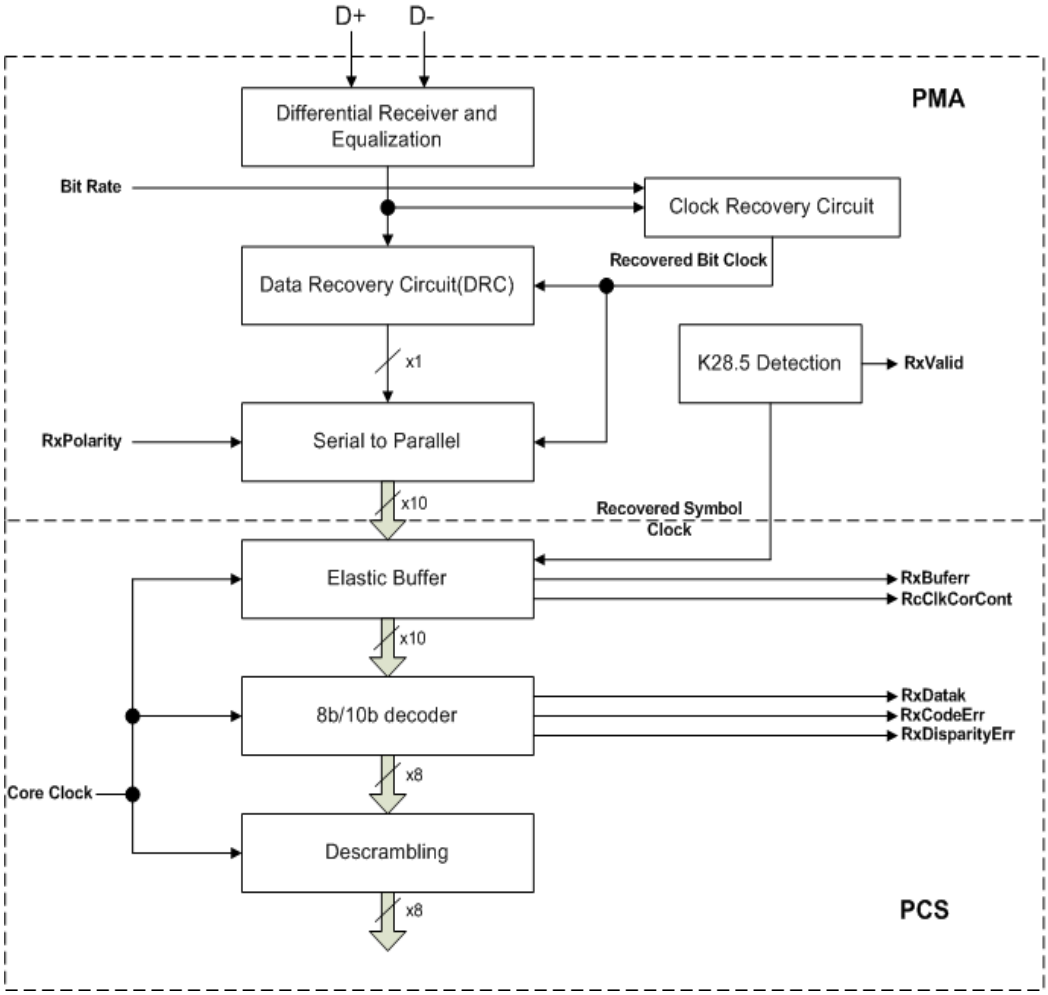

Fig. 4. USB physical layer: Receiver.

5. Verification Modules

The following modules are developed for verification: Receiver, Driver, Monitor and Pseudo Random Data Generator (PRDG). Driver and Monitor can be configured to work in one of the following modes: transceiver and receiver. Below is the description and function of each module.

Receiver– retrieves data from Rx interface of link and stores it in the FIFO. It contains small logic to detect data payload and a FIFO. The implementation of this module is straightforward and is not presented here.

Driver–gets packets from HT and sends it to link in transceiver configuration and executes release credit and other link commands in receiver configuration.Again ithas a small logic to drive linkTx interface signals. Fig. 5 shows the state machine of Driver. After start request driver gets packets from HT. If it is a TP state becomes Hnd_TP. After TP is handled TP_done is asserted state becomes Get_Packet. All packets one by one are taken from HT and the same procedure is done. When all packets are completed Test_complete is asserted and state becomes IDLE.

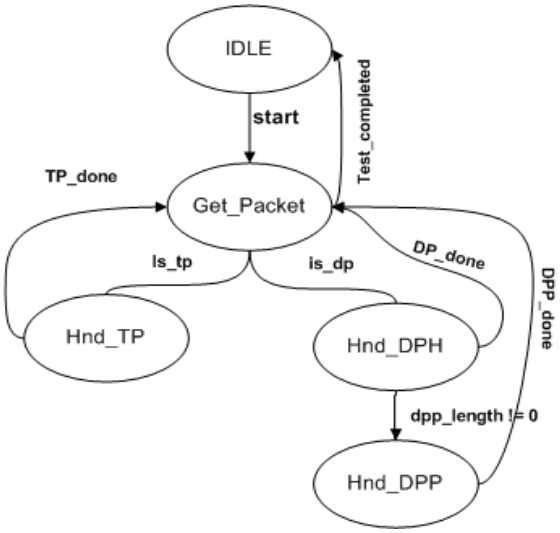

Fig. 5. FSM of the Driver configured as a transceiver.

PRDG – Basically it is a Linear Feedback Shift Receiver (LFSR) which generates 64-bit random data when directed by monitor or driver (for data packet payload). The structure of LFSRs and the seed (initial state) used by transceiver and receiver are the same therefore generated data is the same. This make possible for monitor to verify received data. A simple counter can be used instead of LFSR.

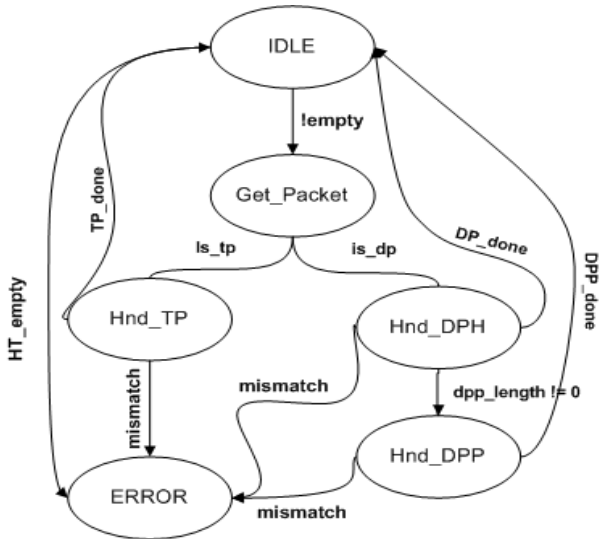

Fig. 6. FSM of Monitor configured as receiver.

Monitor – when configured in receive mode it is connected to PRGD and receiver. In transceiver mode it is only connected to Receiver. In receive mode monitor gets data payload from Receiver and compares it with data generated by PRDG. Assertions for Tx/Rx paths are included in this module. The monitor is most complicated part of verification environment (not included USB3.0 link and PCS). Though Virtex5 is a big FPGA but employing more than 70% of resources will cause tim-

ing issues i.e. will affect performance [9]. This is the reason why it is not possible to implement all needed assertions at once. Only small part of assertion is added. To make monitor smaller Transaction Packet (TP) and Data Packet Header (DPH) parsing is not implemented. It is replaced with a structure which we call Hardware Test (HT). HT is a list of packets which are going to be transmitted by driver. Receiver and transceiver contain the same tests and during initialization the order of HTs which are going to be executed is communicated. During test execution driver gets first packet from HT and forwards it through link and the receiver get packet from link and compares it with the first packet of its own HT. The Monitor FSM is shown in Fig.6. When Receiver FIFO is not empty Monitor get a packet from HT and compares it with received one. If it is a DPH with data length not equal to 0 in Hnd_DPP state it gets data from PRDG and compares with received DPP. In state of mismatch Monitor updates appropriate registers in ERROR state.

6. Lifecycle of the packet

In this section the lifecycle of the packet is described. First the header of TP or DP is taken from HT. Let's assume that is it DP. Driver checks the length of the packet (header contains data length), if it is zero DP is treated the same way as TP. Packet is forward to link which sends the packet to the partner. Receiver detects the packet and pushes it to FIFO. Empty signal of FIFO becomeszero.As we described earlier Monitor detects non-empty condition of receiver FIFO and pops the packet. After that it compares received packet with expected one (from HT). In case of mismatch flags an error. If everything is correct release credit command is executed by Driver and lifecycle of packet completes.

7. Experiment Results

As it was mentioned earlier our environment doesn't include PCs so it is not possible to use currently available benchmarking tools so we have used Ellisys's"USB Explorer 280" to calculate transfer speed. It was connected between link partners by USB3.0 cable. Synopsys Identify is used to sample registers which capture results of the covered assertion and test results. Synopsys's Synplify Premier is used for synthesis, Xilinx's ISE for place and route, bit file generation and Xilinx's Impact to load bit file into FPGAs. The Table 1 shows the utilized resources. As XC5VLX330T is the biggest FPGA in Virtex5 family so this utilization can't cause any timing issues.

	Configuration	
Resources	USB3.0 Link+ PCS + modules for Verification	USB3.0 Link + PCS
DCM_ADV	3	2
PLL_ADV	2	2
RAMB18X2	1	1
RAMB18X2SDP	1	1
RAMB36_EXP	5	5
Slice Registers	3956	2715
Slices	6679	5101
Slice LUTS	9540	7182
Slice LUT-Flip Flop pairs	11523	8312

Table 1. Utilized resources in Virtex5(XC5VLX330T) FPGA

We were able to prove all added assertion related to interface between protocol and link layers. There were no failed assertions because design is fully verified. Implemented assertions were checkedby injecting error conditions (e.g. delayed a signal for one clock cycle). Also we were able to calculate maximum speed of USB3.0 link implementation on FPGA. As our implementation is fully based on hardware so it doesn't suffer from performance limitation of verification system. We were able to reach 442MB/s for Bulk-In transfer (only bulk is supported) and 439MB/s for Bulk-Out transfer.

8. Conclusions

In this article verification environment based on synthesizable assertions, monitor and data generator is presented which addresses challenges described in [1]. Testing is performed at speeds near to theoretical maximum which is described in [4]. The overhead resources of verification modules are smaller than 30% of "USB3.0 Link + PCS" configuration which is acceptable as design of the link layer is not big. Some assertion related to link layer interface protocols (link commands, and basic transfers) were proven. Adding all needed assertion is not possible as resources of FPGA are limited. In future works we'll try to resolve this issue.

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USB IP DEVELOPMENT FLOW BASED ON SYNTHESIZABLE ASSERTIONS

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1. Introduction

The original Universal Serial Bus was developed to be user-friendly plug-play way to attach external peripherals to Personal Computer. The first designs were not big and required reasonable time for verification (e.g., USB1.1). USB has gone beyond a way to connect peripherals to PC. Now, almost every device uses USB for communication. The speed increased from 12 Mbps (USB1.1) to 10 Gbps (USB3.1) and as a result of this the size of the hardware needed to support these speeds (ASIC gate count) increased significantly [1,2]. The number of clock domains has increase from 2(even 1for some USB1.1 configuration) to 6(USB3.1). Various power saving options are added during USB development.The verification burns 70% of design cycle [3]. In order to deliver competitive product all this enhancements must be verified properly.

Standalone verification of the USB design requires hours or even days of simulation time.Typically the USB is used withinSoC as a peripheral interface. Even if USB IP has been designed and fully verified when it is integrated on a SoC many bus transaction problems may occur, such as protocol violation, performance bottleneck and race conditions etc. To be sure that design will be fully compatible with other IPs in SoC it is important to verify that standard interfaces (e.g. AHB or AXI for PCIE) which are used to connect USB to other cores are implemented in accordance to specifications.

Functional coverage is an important quality metrics for IP.The tools which are provided by EDA vendors do not allow automaticcalculation of functional coverage. System Verilog (SV) or Property Specification Language (PSL) assertions are used for that purpose. To verify the design complex simulation environments are developed, but traditional techniques relying on procedural testbench languages are no longer sufficient. Checkers and coverage monitors need to be more concisely specified, especially when describing behaviors that span multiple clock cycles. Bugs need to be more quickly isolated to decrease debugging time. Stimulus generation needs to be further automated to accelerate coverage closure. Assertions enable all these productivity improvements by concisely specifying temporal behaviors for checkers and coverage monitors, pin-pointing bugs closer to their source, and enabling formal model checking techniques to automate stimulus generation [4].

Although System Verilog assertions are good tools for debugging and functional coverage calculation but significant effort and time is spent on simulation to achieve desirable results. A full testing should be performed after every RTL change. Delivering fully verified USB product became complicated and time consuming task.

Prototyping is significantly faster than simulation. For example to run simulation with 1MB Bulk-IN transfer from host to device more than 2 hours are required or testing of power saving capabilities of USB(device or host) consumes more than 4 hours of simulation time, doing the same in prototype consumes not more than 5 seconds.

Although replacing simulation with prototyping is not possible but moving some design verification tasks from simulation to prototyping can decrease verification time significantly.Functional coverage calculation could be performed significantly faster during prototyping than in simulation. But unfortunately System Verilog assertions are not synthesizable.

In this article synthesizable assertion based USB IP development methodology is proposed. Using this flow will make functional verification more effective by facilitatingdebugging failures of FPGA prototype and by allowing calculation of functional coverage for prototyping. Also new methodology allows performing verification of some corner cases by prototyping instead of simulation which will decrease simulation time and help to detect errors which are caused by “real world data effects”.

2. Typical USB IP design flow

The typical USB IP development flow is presented in Fig.1. In this flow verification is mainly performed by simulation. Hardware validation is not considered as a tool for debugging most of failures.

Design Specification – The device, hub or host controller is designed based on specifications provided by USBIF. The design is partitioned (link layer, protocol layer, application communication layer etc.), every part is described individually and the interfaces between the modules are defined. To facilitate debugging and integration defined protocols for interfaces between sub layers are used instead of just a bench of signals. This allows defining assertion for internal interfaces.

Behavioral description -The behavioral model should be simulated in order to verify that the desired functionality is captured completely and correctly. The behavioral abstraction is then used as a reference to create and refine a synthesizable register transfer level (RTL) abstraction that captures the desired functionality required by the design specification.

RTL development - The Register Transfer Level description of USB core is developed during this stage.

Unit Level Test Environment development and testing -This stage should be started in parallel with RTL development. ULTE is developed and testing is performed. It includes System Verilog assertion development, to test functionality of sub

modules, based on test specifications which are provided by USBIF or internally developed. The individual parts of design are tested. Different error injection scenarios are executed. It is easier to reach high assertion coverage values at this stage.
Full TE development and testing - The individual parts of design are integrated and the full TE is developedafter unit level test passing rate reaches to some desirable value. During this stage the assertions for internal (between sub modules) and external (between USB and other cores) interfaces are developed. Simulation time increases significantly and to hit all assertions days are required for simulation.

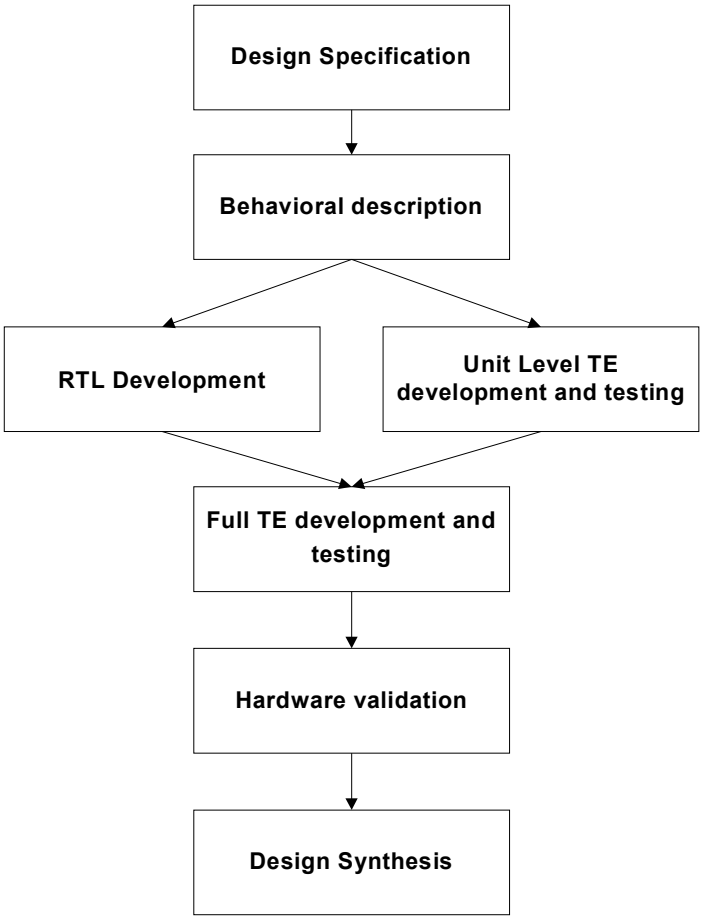


Fig. 1. Typical USB IP development flow.

Hardware validation - The hardware validation is performed by using FPGA prototype. The RTL should be mature so prototype development is started after RTL is functionally verified by simulation.Some modifications are done in RTL to be able to map it to FPGA. For example clock gating can cause overflow of FPGA clock resourcestherefore it should be replaced as described in [5].After all modifications are done and constraints are developed the bit file is generated. Validation is performed based on documentation and tools (USB30CV, xHCICV etc.) provided by USB-IF for USB product testing.
Design Synthesis -The HDL Design Synthesis phase involves using a synthesis tool to:
• Translate the abstract RTL design description to register elements and combinational logic,
• Optimize the combinational logic by minimizing, flattening and factoring the resulting Boolean equations,
• Translate the optimized logic level description to a gate level description using cells from the specified technology
• Optimize the gate level description using cell substitution to meet the specified area and timing constraints, and
• Produce a gate level netlist of the optimized circuit with accurate cell timing information.
HDL Design Synthesis finishes with "post-synthesis" simulations to verify that the gate level circuit fully provides the desired functionality and meets the appropriate timing requirements.

3. System Verilog assertion

An assertion is a statement which describes the intended behavior of a design. It ensures consistency between design intent and implementation.

Traditional verification approaches rely on injecting random stimulus into the design under test and measuring the output. However the complexity of design increases which makes coverage and debugging much harder. Assertions can help to improve verification in following ways:

- Concisely express behaviors that span multiple clock cycles,
- Provides a mechanism for precise documentation of design and assumptions,
- Improves observability of internal interactions,
- Pinpoint errors at the point of origin,
- Provide a mechanism to track coverage.

System Verilog Assertions (SVA) language provides a set of constraints that can be usedwithin Verilog 1995/2001 and System Verilog. Simple events or complex temporal sequences of event can be detected with SVA.SVA assertions can be used inside synthesizable design blocks as well as inside behavioral testbenach blocks. Immediate and concurrent assertions are supported by SVA. Immediate assertions are event driven and procedural in nature. The Boolean expressions are executed immediately rather than at clock edge. Immediate assertion are used in always and initial blocks.

For example this statement can be used in USB host transceiver side to check if device receiver's buffer has available space to be able to handle packet and fails when space is not available and packet is accepted.

```
assert (numer_of_remote_credits != 0) $display ("Packet is accepted");
else $error("Packet accepted when there are no credits").
```

This assertion should be used within transceiver state machine.

Concurrent assertions allow functionality over time to be specified**.**This is an example of simple sequence which is used for concurrent assertion. It checks if the header sequence number advertisement request is issued when link state becomes U0.

```
sequence entry_to_u0_initialization1; @(posedgeclk)
!entry_to_u0 ##1 entry_to_u0
##1 tx_advert_rqst;
endsequence
svc_u3link_tctrl_entry_to_u0_initialization1: cover property (entry_to_u0_initialization1)
$fdisplay(file1,"SVC: 7.2.4.1.1_2    svc_trans_entry_to_u0_initialization1      at time %0t",$time).
```

The example assertions above are developed based on Link Layer Test Specification [8]. It is straightforward task to translate this assertion to synthesizable RTL code which can be used within prototype. The assertionmode shouldbe instantiated within the transceiver. Using this type of assertion requires certain effort as it is inside RTL and status signal should be taken to the top module.

This assertion is used between PCIE and USB controllers to check AXI interface implementation.

```
sequence s_axi_aw32_access;
@(posedgegm_clk)
xm_awvalid ##0 (xm_awaddr< 64'h0000000100000000) ##0 xm_awready;
endsequence
sva_axi_aw32_access: cover property (first_match(s_axi_aw32_access))
$display ("SVCL: sva_usb3_axi_aw32_access at time ",$time).
```

It checks if 32-bit write access happens. Almost on effort is needed to add this assertion as the synthesizable RTL for this assertion is instantiated within FPGA top module.

4. Example of synthesizable assertion for USB

In this section implementation of synthesizable assertion is described for USB root hub. It checks if port state machine goes to PRT_RESET after global reset and then after one clock cycle prt_dbc_pr is asserted.

```
property port_rst;
@(posedgeclk)
  (reset_request) ##[1:3] ($past(fsm_prtsm) != PRT_RESET)&& (fsm_prtsm == PRT_RESET) ##3prt_dbc_pr;
endproperty
svc_u31prt_dbc_port_reset: assert property (port_rst)
  $fdisplay(file1,"[%0t ps] SVC: rhb_prt DBC enters reset in 2 clocks",$time).
```

The FSM which should be implemented is described in Fig. 2. It has reset_request, fsm_prtsm and prt_dbc_pras inputs and status complete as output signals. At the beginning after reset the state is IDLE. After first event happens state becomes W4PRTRST. In this state it wait for second condition from 1 to 3 clock cycles, and if it does not happen during that period assertion completes with fail status. After second conditions passes state becomes W4PRTDBCPR. The passed status is asserted in DONE state. The implementation is similar to synthesizable assertions described here [7].

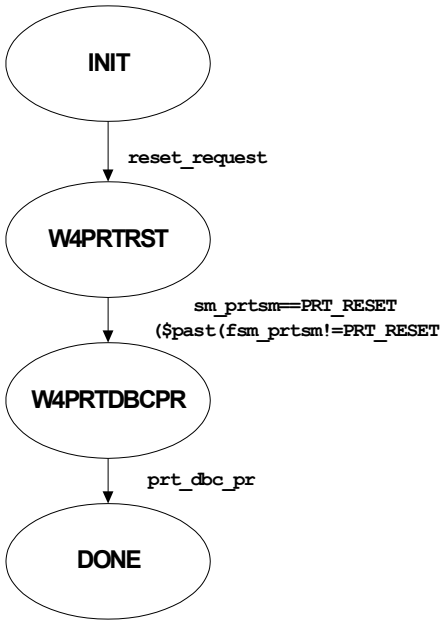
5. Proposed methodology

FPGA prototyping enables testing of USB core at speeds close to ASIC and with high accuracy [6]. The main reason to prototype is "interfacing with the real world" and prototyping offer fastest and most accurate way to do that in advance of real silicon becoming available. The main drawback of prototyping is lack of visibility. It is possible to instrument an FPGA in order to gain some visibility into the design's functionality, but even the most instrumented design offers only a fraction of the information that is available in an RTL simulator.

As you can see in Fig.3 some new stages are added and therefore engineering effort is increased. Significant amount of work is done to develop, test and integrate assertion, but once it is done the environment is highly reusable for different revisions of USB core. The first two and the last stage are not changed, other stages are described below:

Development of Synthesizable RTL for assertions- The assertion RTL and core to support result retrieval (numbers of passed and failed assertions) and assertion configuration (e.g. enabling or disabling specific assertions) are developed.

ULTE development and testing - As you can see from diagram the development of RTL, ULTE and assertions could be started simultaneously. The testing of assertion RTL **i**s added to tasks performed in the same stage of typical flow. Some testing methodologies are described in [6].




```
module port_rst(fsm_prtsm,reset_request,prt_dbc_pr,
                                        clk,reset,status,complete);
//IO declarations
...
reg   [1:0] fsm_prtsm_d,cur_state, next_state, count;
parameter PRT_RESET = 2'b1;
…
always @(posedgeclk) begin
        if(reset) cur_state<= IDLE;
        else  cur_state<= next_state;
end
always @(*)
case(cur_state)
IDLE:
If(reset_request)  next_state = W4PRTDBCPR;
W4PRTDBCPR:
begin
if(conut<3) begin
if(fsm_prtsm_d != PRT_RESET &&fsm_prtsm ==PRT_RESET)
next_state =W4PRTRST;
end else
begin
complete = 1'b1;
status   = FAILED; …
end
W4PRTRST:
begin
        ...
end
DONE:
begin
complete= 1'b1;
status= PASSED;
next_state= IDLE;
end
endcase
```

Fig. 2. FiniteState machine for port_rst assertion and Verilog implementation.

Full TE development and basic testing - As it was mentioned earlier prototyping cannot replace simulation therefore the Full TE should be developed to be used in current and other stages of design, but the number of tests cases could be decreased. After testing connectivity and running some basic transfer tests it is possible to start FPGA prototype development due to added visibility provided by assertions.

FPGA prototype development and integration of synthesizable assertion – In this stage the FPGA prototype is designed and modules for assertion support are instantiated in FPGA (assertion for external interfaces and support) and the USB controller (assertions for internal interfaces and new ports for result retrieval) top modules.

Simulation – This stage is needed because basic testing is required after every update in RTL.

Hardware validation - The same validation is performed here but debugging is easier because the ability to analyze the inside of a design i.e. being able to access signals, registers and the state of the hardware design. Also prototyping functional coverage is calculated.

6. Conclusions

The proposed methodology can be used to facilitating failure debugging in prototype as well as make possible to calculate functional coverage for prototyping. It is possible to remove the tests that were user for functional coverage from simulation and thought decrease simulation time. The prototyping can be started after running basic tests to check connectivity and simple data transfers which will decrease time to market.

Thought this methodology is improving verification process but there are some issues, which should be taken into account. First, significant engineering effort is needed to develop, test and integrate synthesizable assertions and control logic within prototype. This issue can be solved by developing synthesizable assertion libraries and testing it with good known USB designs. These libraries can be reused by different USB developers. Second, as we know the FPGA resources are limited therefore it is not possible to use all needed assertions at the same time. To solve that issue partial reconfiguration feature of FPGA can be employed. These and other issues will be investigated in future works.

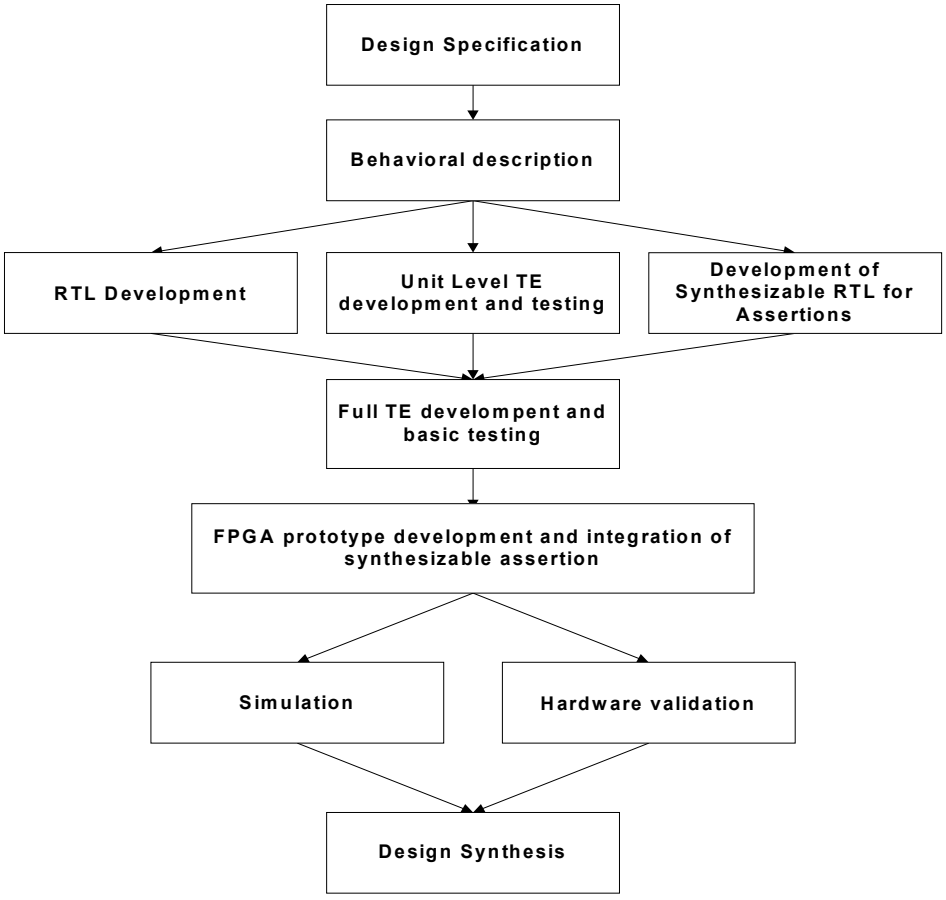


Fig. 3. Proposed USB IP development flow.

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DIGITALLY ADJUSTABLE NON-OVERLAP CLOCK GENERATOR FOR SWITCHED-CAPACITOR CIRCUITS

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1. Introduction

The progress of VLSI systems stimulated emergence of many novel approaches such as switching capacitor circuits, dynamic and clocked logic gates, which provide high speed data processing with low power dissipation [1]. Non-overlap clock generators (NOCG) are widely used in modern switched-capacitor (SC) circuits, particularly in power converters, to operate the switches and minimize the charge losses in flying capacitors [2,3]. Being a part of control block of SC converters, the NOCGs must meet the specific requirements to assure overall efficiency and stability of the system. The most significant of those requirements are non-overlap period (NOP) stability of dual phase output signals over supply voltage variations, low output signal jitter and near 50% duty cycle [4].

Conventional NAND/NOR based NOCGs are using inverters as delay cells to form the NOP of dual phase output signals (Fig. 1). This approach is beneficial when dealing with high frequency applications, where the NOP is small compared to the input clock period [5]. The SC circuits require relatively lower processing frequencies, as well as adjustable NOP to control the system characteristics. For these applications, the conventional structures fail to meet the basic requirements in several aspects. First is the unacceptable increase of inverter count in the delay chain in order to provide sufficient delay interval to form the required NOP. This causes unacceptable increase in power consumption, another factor, which restricts the usage of conventional structures. Furthermore, in NAND/NOR based NOCGs the NOP is constant and depends on the number of inverters used in the delay chain, which cannot be modified for particular design. Taking into account above-mentioned issues, a new design is proposed, which provides two-phase non-overlapping clock signals with digitally adjustable NOP.

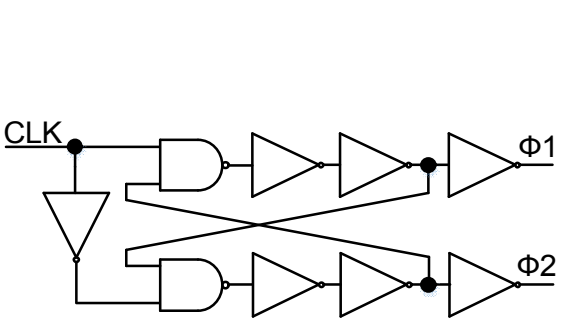


Fig. 1. Conversion block of fractional ½ SC converter.

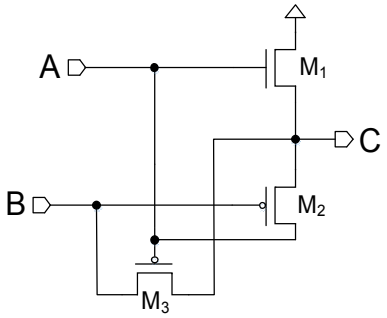


Fig. 2. Three transistor XOR gate.

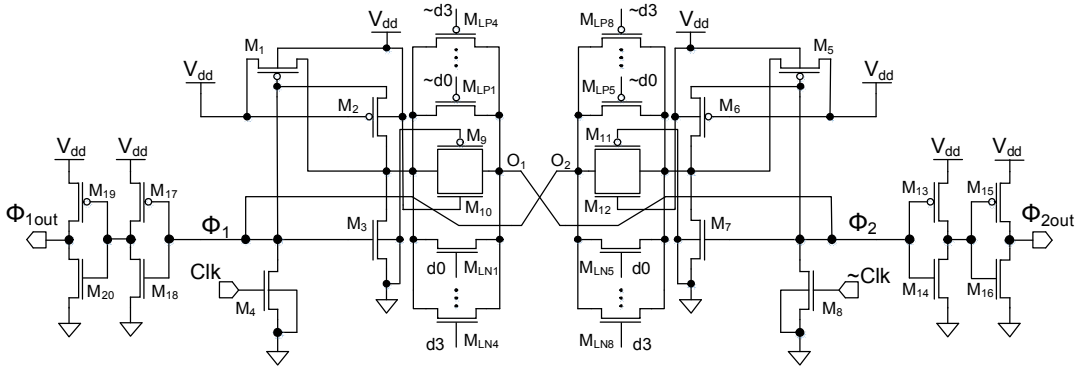


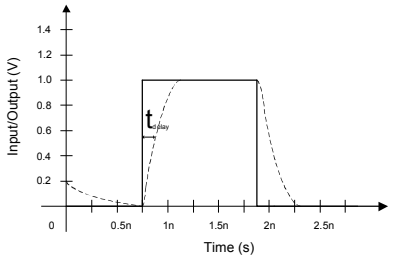
Fig. 3. Proposed non-overlap clock generator.

2. Structure of proposed non-overlap clock generator

The proposed design is based on novel three transistor XOR gate (Fig. 2), which consists of two PMOS and one NMOS transistors [6]. When the input B is at logic high, the structure works as a simple inverter. Structure of designed NOCG is shown in Fig. 3. A back-to-back structure is used to generate dual phase non-overlap output signals [7]. Input clock signal is given

to the gates of NMOS pair M4, M8. A VDD voltage is given to M2 and M6 PMOS transistors, which assures their OFF state throughout the switching period. With this configuration, VDD and ground rails are separated to lower the dynamic power consumption. The output nodes of each stage are charged through VDD-M1/M5-TG-O1/O2 path and discharged through O1/O2-TG-M3/M7, which means no direct path from VDD to GND is present during the switching process.
Besides the XOR gates, transmission gates (M9-M12) also participate in the formation of output signals, with bringing their own delay (1) to form the initial state of NOP (Fig. 4).

$$t_{delay} = 0.7\,(R_n||R_p)C_{load}, \tag{1}$$



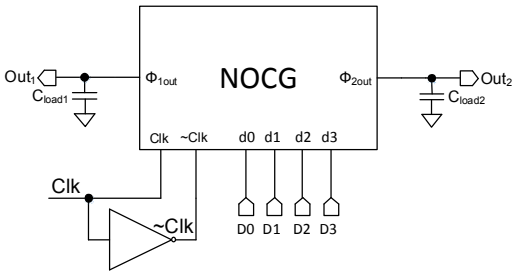


Fig. 4. Operation of transmission gate [1].Fig. 5.Simulation circuit of proposed NOCG.

To control feedback chain delay, 4 NMOS-PMOS pairs are connected in parallel to the transmission gates. Each pair is controlled by corresponding digital signal (d0-d3). By manipulating the count of open pairs, the overall effective resistance of transmission gate is modified (2 and 3), thus adjusting the NOP.

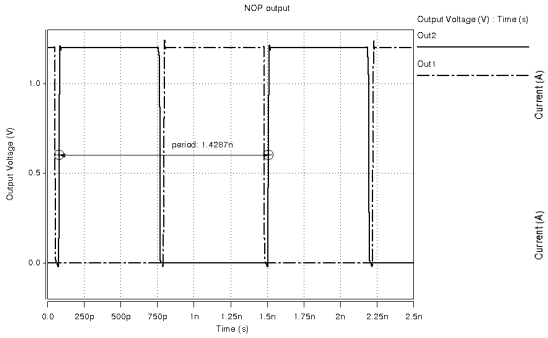
$$R_p = \frac{VDD}{\frac{KP_p}{2}*\frac{(W_p+d0*W_{lp1}+\ldots+d3*W_{lp4})}{L}*(VDD-V_{THp})^2}, \tag{2}$$

$$R_n = \frac{VDD}{\frac{KP_n}{2}*\frac{(W_n+d0*W_{ln1}+\cdots+d3*W_{ln4})}{L}*(VDD-V_{THn})^2}. \tag{3}$$

As the output voltage of NOCG can vary depending on the values of control voltages and supply voltage of NOCG itself, additional inverters are used for both output phases to ensure rail-to-rail bandwidth of output signals as well as to increase the driving capability of the circuit (M13-M15). Overall structure of proposed design with load capacitances and input voltage sources is shown in Fig. 5.

3. Simulation Results

Proposed NOCG is designed using CMOS 32nm SAED technology. Fig.6 shows two phase non-overlap output signals of proposed NOCG working with input clock frequency of 700MHz and with 1.2V power supply voltage. A NOP of 61ps is obtained in case of 0000 configuration of 4 bit digital control signal. To provide similar 61ps of NOP, a conventional NOCG with delay line of 18 inverters is used, thus making the proposed design more efficient in terms of used transistor count, as similar NOP time is obtained using only 36 transistors compared with 82 transistors used in conventional NOCG.



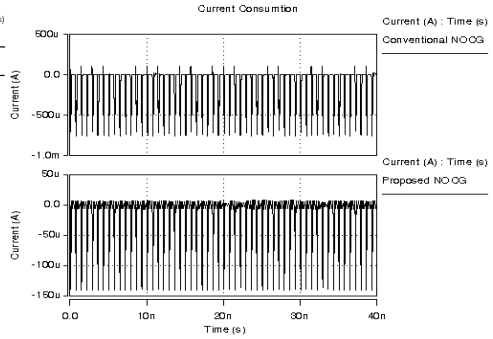


Fig. 6. Two phase output voltages of proposed NOCG. Fig. 7. Current consumption of proposed and conventional NOCGs.

The current consumption of both conventional and proposed designs is illustrated in Fig. 7. As the proposed structure doesn't have direct current path from VDD to ground, the maximal current pulse value reaches up to 140 uA for 1.2 V of supply voltage. In case of conventional NAND based NOCG, a shoot-through current is present during input signal rise and fall periods when both NMOS and PMOS transistors of the inverter are open. Moreover, as the overall consumed current of con-

ventional NOCG is the summary of all inverters used in the delay line, which leads to consumption of larger currents (reaching up to 0.8mA in simulated case).

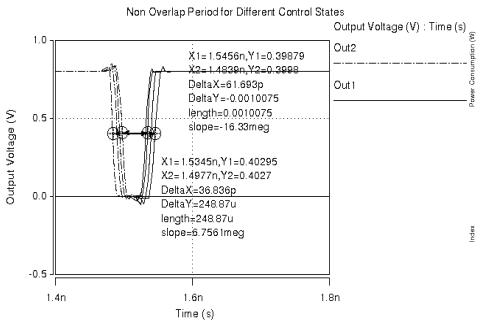


Fig. 8. NOP variation depending on digital control value.

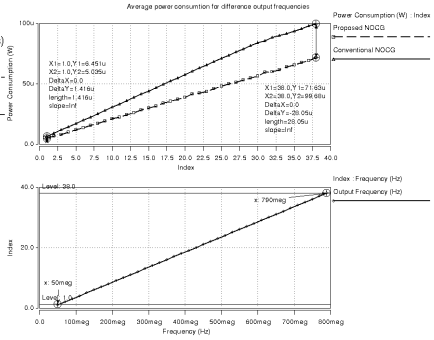


Fig. 9. Average power consumption of proposed and conventional non-overlap clock generators.

NOP variation for 4 different control signal combinations is presented in Fig. 8. NOPs of 36.8ps and 61.9ps correspond to 0000 and 1111 configuration of d0-d3 digital control signal. This is the maximal amplitude of NOP for proposed structure, which is sufficient for the most of the applications. Comparison of average power consumed by proposed and conventional NOCGs during 100ns is showed in Fig. 9. Simulation was performed for input clock frequency varying from 50MHz to 800MHz. In proposed structure, as shoot-through component of consumed current is much less than in conventional structure, there is less variation of consumed power with regards to output frequency. Although power consumption of the two structures are similar for low frequency applications, when considering overall consumed power for total frequency bandwidth, the proposed structure demonstrates better low-power characteristics.

Another crucial requirement for NOCGs is stability of characteristics towards environmental condition changes as supply voltage. The sensitivity of output signal NOP to variation in supply voltage for proposed design is shown in Fig. 10. As it can be seen from the diagram, NOP is changed from 21.78 ps to 68.7 ps when supply voltage varies from 0.7 V to 1.2 V, but NOP stays relatively constant for supply voltage change from 1.0V to 1.2V showing 5ps NOP ripple. As the supply voltage in majority of modern low-power systems varies in the specified interval, it can be said that the proposed structure provides acceptable deviation of NOP in both multi-voltage applications and in cases of large supply noises.

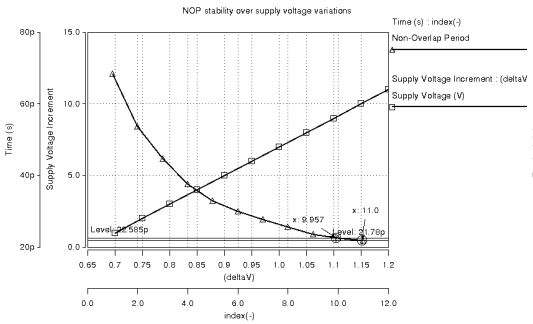


Fig. 10. Non-overlap time stability from supply voltage.

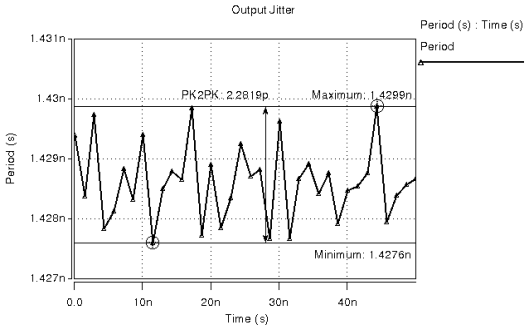


Fig. 11.Output signal jitter measurement.

One of the main sources for uncertainties in SC circuits is the clock signal jitter. Therefore all devices which are located on clock signal generation and distribution path must be designed and optimized to provide low jitter noise and constant duty-cycle of output clock signal. In order to measure the output jitter level of proposed NOCG, pulse widths of output signals are measured during 50 ns time period for 700MHz input clock frequency. As shown in Fig. 11 maximal deviation amplitude of pulse widths during simulation period is 2.28 ps, which is 0.16% from actual pulse width, which is acceptable for the most of possible applications.

Table 1 shows the performance comparison of proposed NOCG with similar designs in the literature. As it can be seen, the proposed structure shows less average power consumption, while providing wider permissible supply voltage range. Moreover, current design is more stable to supply voltage variations.

4. Conclusions

An energy-efficient non-overlap clock generator on three transistor XOR gates is proposed and the respective circuit designed. Designed NOCG provides digitally adjustable non-overlap period with fewer number of used transistors. An ac-

ceptable stability over supply voltage variations and low jitter level around 0.16% of the pulse width is obtained. Core structure ensures similar rise and fall times for output signal ensuring 50% duty cycle.

Table 1. Performance comparison of the designed NOCG with similar designs in the literature

Parameter	Proposed Design	Conventional Design	[8]
Supply Voltage (V)	0.8-1.2	1.2	1.2
Current Consumption (A)	50u	90u	-
Peak Current (A)	110u	0.8m	-
Average Power Consumption at 100MHz (uW)	18.2	37.4	34.47
Cload (pF)	5	5	-
Maximal Output Frequency (MHz)	950	1200	100
Technology (nm CMOS)	32	32	180

Acknowledgements

Design was implemented using SAED 32/28nm EDK [9] developed by Synopsys Armenia Educational Department. Synopsys tools Design compiler and IC Compiler provided by Synopsys Armenia Educational Department.

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THE NEW METHOD DEVELOPMENT FOR THE CONSRUCTION OF LOW POWER CONSUMPTION DECODERS

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1. Introduction

ModernVLSI-sarefrequently usedblocksofstorageand memory devices. Static random access memory (SRAM) devices block diagram isshown below (Fig. 1).

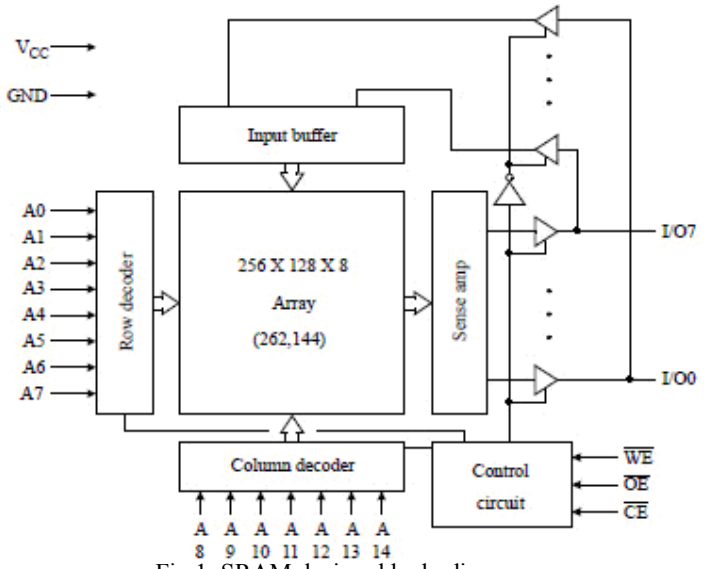

Fig.1. SRAM devices block diagram.

A significant problem in the design of SRAM is the increase of high-speed and decrease of consumptionpower. SRAM consists of rows and columns decoders, sense amplifier, input data buffer, memory array and control circuit. The input data buffer servesfor data classification and management. Sense amplifier serves as collector of information for thereaders. The information is stored in the storage battery cell through two inverters (Fig. 2).

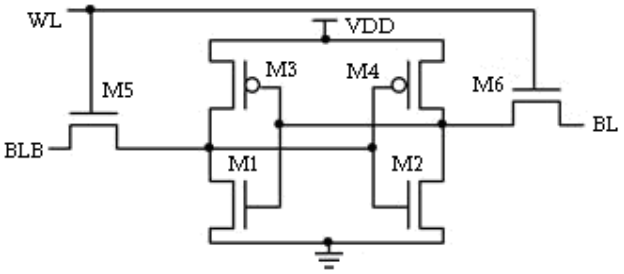

Fig.2.Basic circuit 6T memory cell.

In Fig.1 the memory array represents 8 parallel sectors, which consist of 256 rows and 128 columns.The control circuit realizes reading and writing operations in the memory.Row and column decoders are designed for the cell selection from thecollector, in which information must be recorded or read.The decoder isthe main block of SRAM on which up to 50% access time of memory cell and up to 40-45% of power consumption are spent in normal writing and readingoperations.For the design of address decoder two important factors are to be considered.

1. Select the right structure decoder.
2. Make the right choice for the size of transistors.

The work goal is to develop a new method for construction of decoders which will provide low power consumption and small delay time. SRAM's work beginswiththe decipherof the address. SRAM performance depends on the time necessary

for proper cell selection for the address storage cost and power consumption during that period The.decoder output signal is described by the following formula:

$$y_i = \begin{cases} 0, & i = k; \\ 1, & i \neq k; \\ k = 2^{n-1} \cdot x_{n-1} + \ldots + 2^1 \cdot x_1 + 2^0 \cdot x_0 \end{cases}$$

2. Theory

Linear decoder provides the smallest delay time for code modification, but sequence revenue growth increases the value of the load. For that purpose the decoder is implemented by a multi-level pyramid structure, which leads to additional revenues doubling each subsequent cascade of exits. Therefore, the delay time at the pyramid structure will be a large number of cascades.Let's consider 4 input (a0, a1, a2, a3) and $2^4 = 16$ output (q0 - q15) linear decoder on the logical cells AND and NOT (Fig. 3).A two- input AND element is selected because theincrease of inputnumber brings essential increase of delay time.It is known that AND element is implemented in CMOS technology bymerging NAND and NOT elements.This structure leads to a growth in the number of transistors, thus increasing the delay time and power.Apart from these drawbacks,such structure decoder has one significant shortcoming, the risk of false signals, as a0, a1, a2, a3 inputs(Figure 3) spread in different ways, which also brings an additional increase in power consumption.In this work the layout design of a decoderpresented in Fig. 3 is donewith the help of Custom Design software tool (Fig. 4), on the basis of netlist (description) resulted from it, the modeling is done by software tool in Hspice (Fig. 5).For the development of a low power consumption decoder,a true table for logical cells AND, OR, NOT and NOR, NANDin table 1 is given [1-6].

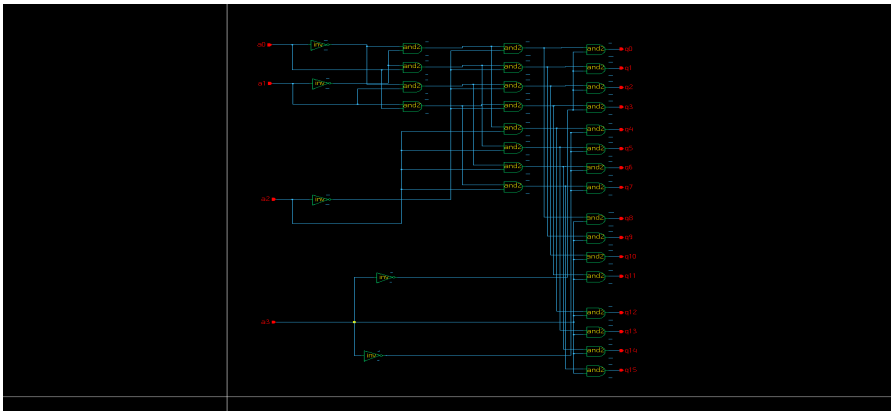

Fig.3. 4 input 16output linear decoder circuit.

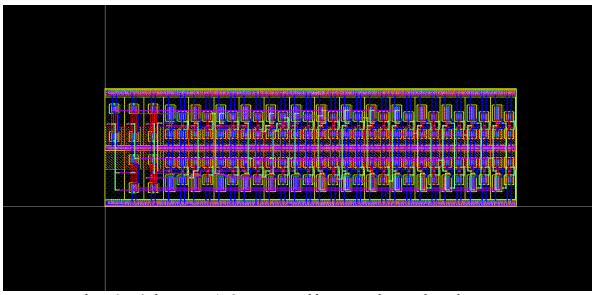

Fig.4. 4 input 16output linear decoder layout.

Table 1. True table AND, OR, NAND, NOR cells

Input value		Output value			
A	B	AND	OR	NAND	NOR
0	0	0	0	1	1
0	1	0	1	1	0
1	0	0	1	1	0
1	1	1	1	0	0

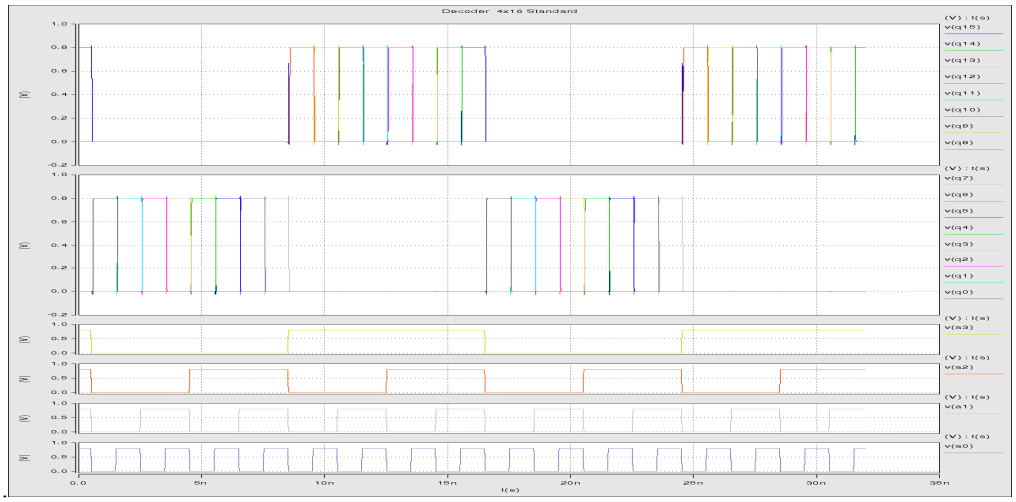

Fig. 5. 4 input 16output linear decoder simulation results on Hspice

Table 1 shows that only at input logic combination 11 in the NAND logic cell exits logic 0 from any combination of the input , in other cases it turns out exit 1.In the case of NOR cell combination of an exit from the 00: 1, while in other cases it turns to 0.From this it is evident that the NAND and NOR logical combination of the elements it will be possible to avoid extra inverter cells, which will increase capacity and delay time.For that, it is necessary to use a combination of two simple principles:

1.If it is necessary to output logic high level (1) of the cascade apply NOR cell considering table 1 data.

2.If it is necessary to output logic high level (0) of the cascade apply NAND cell considering table 1 data.

These two principles make it clear that if we know at least one of the required output signal cascades (logical cell NANDor NOR), the next and previous cascade elements are also known.

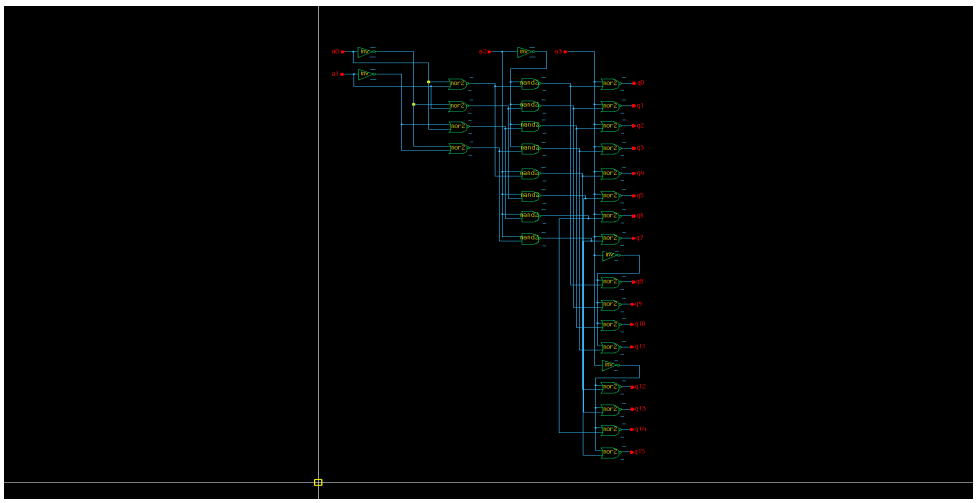

Fig. 6. 4 input 16output decoder on the NAND and NOR cells.

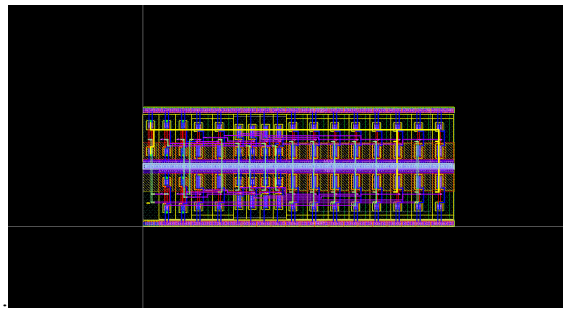

Fig.7. 4 input 16output decoder on the NAND and NOR cells layout.

For example, if it is known that the n stage decoder should be the logical outcome of a high level, it implies that the cascade NOR element must be used according to the 1st principle.Consequently, the n-1 and n + 1 stages NAND logic cellwill be used.By this logic all the cascadesof a decodercan be built.Using the above observations and proposed two principles we will create decoders 4x16 on NAND and NOR logic cells (Fig. 6).The main drawback of such structure decoder is thatit is not fully optimized according to the number of transistors, delay time and power consumption, as well as the danger of false signals. For this structure a design layout iscreated in Custom Designer (Fig. 7). On the generation of netlistextrac,t simulation is carried out in Hspice (Fig. 8).

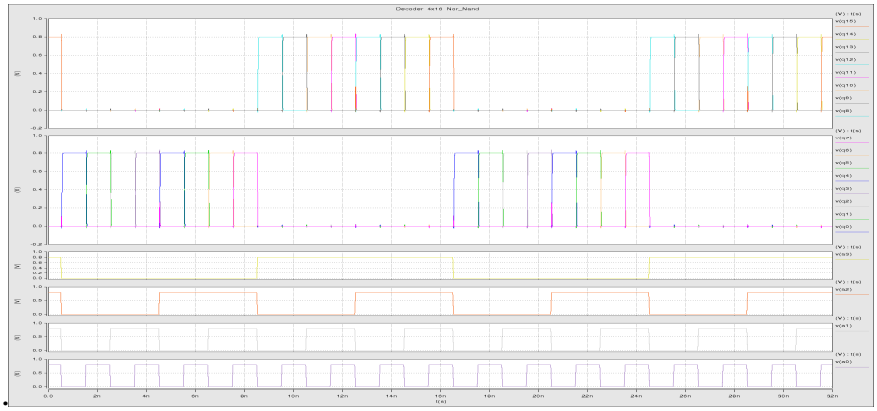

Fig.8. 4 input 16output decoder on the NAND and NOR cells simulation results on Hspice.

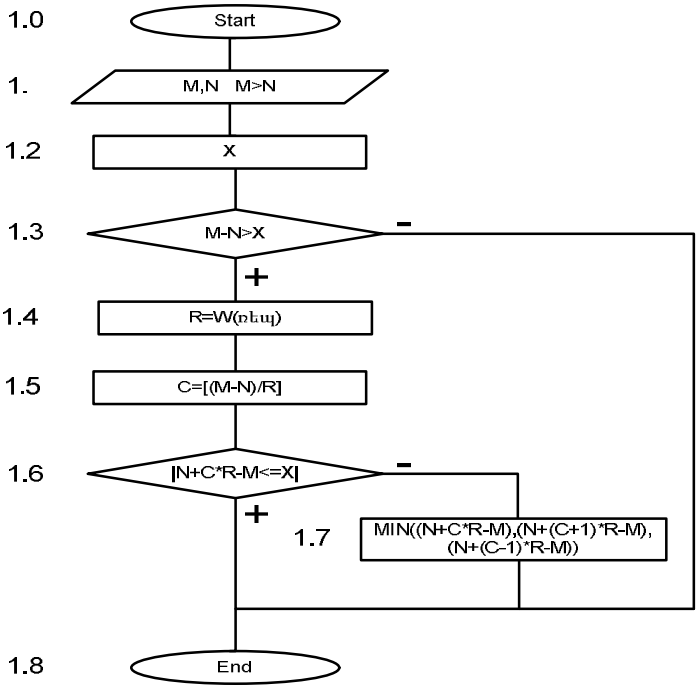

Fig. 9. Algorithm new method.

For the elimination of these shortcomings ithas been suggested to use predecoder structure and inverters replicas increase new method offered by us, the algorithm is presented below(Fig. 9).

1.0 Start

1.1 We have two different ways, which have the active switchingsW(1)=M, W(2)=N.

1.2 The threshold value is defined t = X, which depends on the technology and can be changed at 0.1-0.5 range. Threshold value for optimization is an important component of the scheme.

1.3 Once this condition has occurred W (1) -W (2)> t or (MN> X) and smaller (shorter) on the way inverters replica is added, otherwise no optimization of a difference of ways is made

1.4 The couple inverters switching activity is counted R = W (replica).

1.5 The amount of inverters replica pairs is counted: C, C = (W (1) -W (2)) / W (replica) at dividing, the whole part is taken

1.6 On a short way, C number of replica isadded and thefollowing condition is checked, | (N + C * W (Rep) - M | <= X satisfied end.

1.7 Otherwise,in a short way the number of C-1 and C + 1 replica is added. From the observed three options,that with the smallest difference is chosen.

End

The new structure 4x16 decoderis designed in Fig. 10, the layout and modeling results are shown in Fig. 11 and 12.

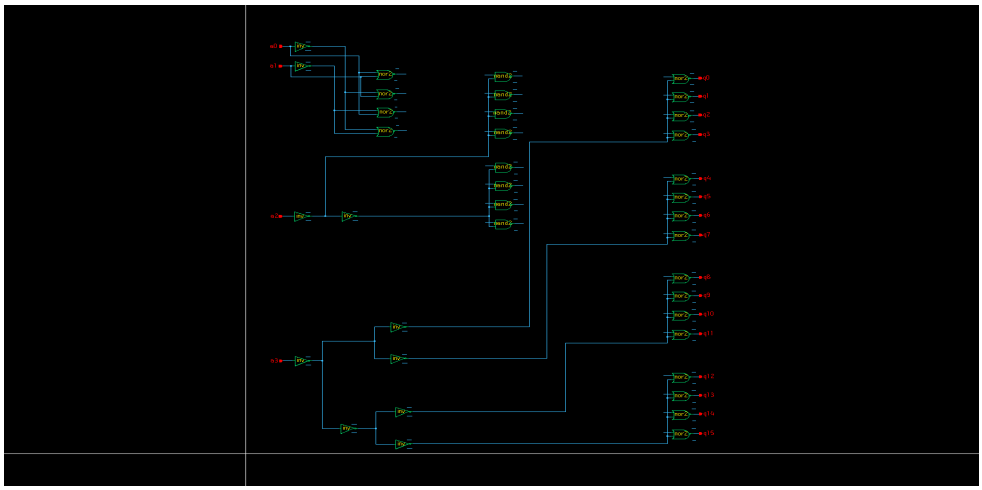

Fig.10. New design decoder 4x16.

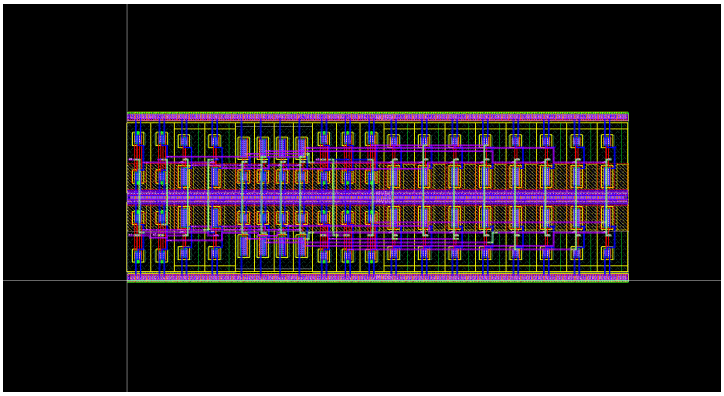

Fig.11. New design decoder 4x16 layout.

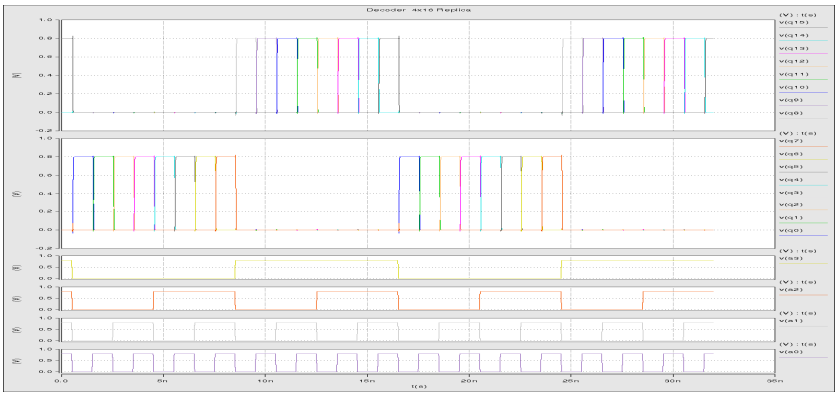

Fig.12. New design decoder 4x16 simulation results.

Figure 12 shows the youngest and senior bit signals q0 and q15 of the three decoders. False signals are taken into red rings.As it is shown in Fig. 13the biggest false signal is derived from the standard structure decoder (Fig. 1), the second biggest false signal is derived from structure decoder on NAND and NOR (Fig. 6). False signalsin thepredecoder and invertores replica (Fig. 10) structure decoder arenot found .

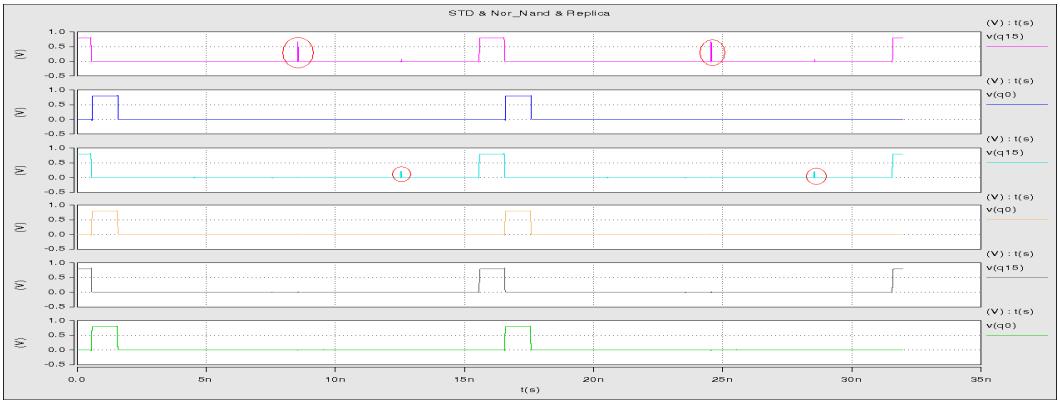

Fig. 13. Showsbit signals q0 and q15 of the three decoders.

Ttable 2 shows that simulation results for high and low bits for three decoder versionsdepend on process-voltage-temperature.

Table 2. Results simulation

Scheme	Process Voltage Temperature	Delay low high q0 (ps)	Delay high low q0 (ps)	Delay low high q15(ps)	Delay high low q15 (ps)	Power (uW)	Area (um^2)
Fig. 3	Typical 0.8v, 25°C	69.54	70.21	59.81	28.93	39.904	125.9
	Slow 0.8v, -40°C	96.99	98.63	82.58	38.36	33.92	
	Slow 0.72v, 125°C	91.01	93.54	78.75	35.47	31.7304	
	Fast 0.88v, -40oC	54.42	54.54	46.43	24.2	50.8288	
Fig. 6	Typical 0.8v, 25°C	49.5	46.88	53.24	30.81	27.488	124.1
	Slow 0.8v, -40°C	69.13	63.18	75.3	41.54	23.28	
	Slow 0.72v, 125°C	63.59	61.64	70.09	38.53	21.8736	
	Fast 0.88v, -40oC	39.66	37.16	41.35	25.26	35.2088	
Fig. 10	Typical 0.8v, 25°C	54.11	52.47	59.78	47.32	31.8	134.1
	Slow 0.8v, -40°C	76.17	69.99	83.2	65.42	26.648	
	Slow 0.72v, 125°C	69.61	68.92	78.49	61.13	25.38	
	Fast 0.88v, -40oC	43.11	41.68	46.57	37.67	40.5152	

3. Conclusions

1. A new method for the creation of decodershas been developed, which provides low dispersion delay time, rules out false signals (power consumption reduction).

2. A schematic layout of three type decoders and simulation is carried out.

3. A comparison was made

While comparing the second decoder tothe firstone, the below results are received:

- Low bit decoder (q0) gains a delay of 27-30% low-high, high-low 31-35%.
- High bit decoder (q15) gains a delay of 8-10% low-high, high-low loses 4-8% (for the reason of signal propagation in different ways).
- Power gain 30-31%
- Area gain1.42%

While comparing the third decoder to the second

- Low bit decoder (q0) delay losses of 8-10% low-high, high-low 10-12%.
- High bit decoder (q15) delay losses of 10-12% low-high, high-low 49-58% (for the reason of signal propagation in different ways).
- Powergain 14-16%
- Area gain 8%

While comparing the third decoder to the first

- Low bit decoder (q0) gain in delay 20-23% low-high, high-low 23-29%.

- High bit decoder (q15) delay losses of 0.3-0.75% low-high, high-lowgains 55-72% (for the reason of signal propagation in different ways).
- Power gain 20-21%
- Area losses 6.11%

The modeling results indicate that the first version is the worst option from the viewpoint of power, delay time and false signals.The second option is the best in terms of power and area.The third option built by the developed method is the best in terms of time dispersion delay and absence offalse signals.

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CMOS MASTER SLAVE FLIP-FLOP FOR LOW POWER APPLICATIONS

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1. Introduction

General D flip-flop is essentially a delay flip-flop and it is so called because the bit at the input is transferred at the output of the flip-flop when the next clock pulse comes. The D flip-flop (figure 1) can be constructed using either SR flip-flop (figure 2) of JK flip-flop. By looking at the middle two conditions of these flip-flops, it will be found that the inputs are dissimilar if one is 0 then the other is 1 and when clock is applied the dissimilar inputs are passed on to the output. This can be done here by placing an inverter in between the two inputs of the AND gate. It is subject to problem called metastability, which can happen when two inputs such as date and clock or clock and reset, are changing at about same time. When the order is not clear, within appropriate timing constraints, the result is that the output may behave unpredictably, taking many x after clock pulse (hold time) [1]. Depending on the flip-flop's internal organization, it is possible to build a device with a zero (or even negative) setup or hold time requirement but not both simultaneously.
Edge triggered register structure is proposed to overcome this issue. The most common approach for constricting edge triggered register is to use master-slave configuration shown in Fig. 3.

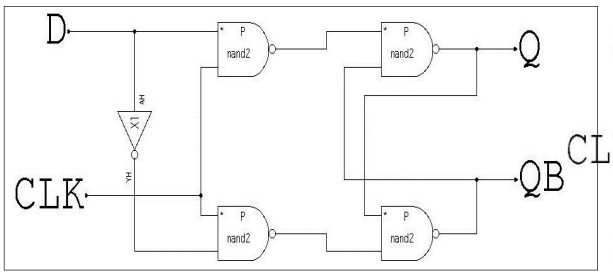


Fig. 1. Block Diagram of D flip-flop.

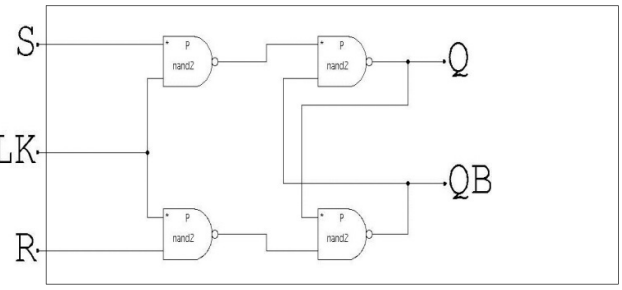


Fig. 2. Block Diagram of S-R flip-flop.

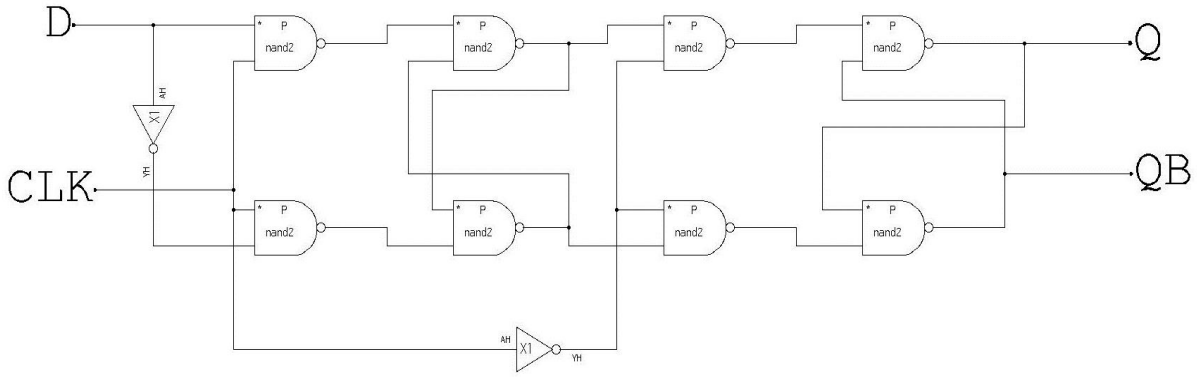


Fig. 3. Block diagram of master slave D flip-flop.

Master Slave flip-flop is enhanced version of general D flip-flop. Two flops are used, the first as master and the second as a slave. When clock pulse is a high, Master Slave flip-flop is active and when it is low, Slave flip-flop is active. Master-Slave flip-flop [4,5,8 ,10] is edge sensitive opposed to D flip-flop which is level sensitive. The main advantage of Master Slave flip-flop is its ability to remove false triggering. It stores two bits in a single circuit. The data transfer from D input to Q output occurs on the negative/positive-going (HIGH-to-LOW/LOW-to-HIGH) transition of the clock input. The D input can acquire new status when the clock is inactive, which is the time period between successive HIGH-to-LOW transitions. The D flip-flop can provide a maximum delay of one clock period [2]. The flip-flop has two types of inputs: Synchronous and Asynchronous. The effect of Synchronous inputs on the flip-flop output is synchronized with the clock input. R, S, J, K and D inputs are all synchronous inputs. The operation of asynchronous inputs does not depend of the synchronous inputs and the input clock signal. These are override inputs as they force the flip-flop output to go to a predefined state irrespective of the logic status of the synchronous inputs. PRESET and CLEAR inputs are asynchronous inputs. When active, the PRESET and CLEAR inputs place the flip-flop Qoutput in the '1' and '0' state respectively. Usually, these are active

LOW inputs. When it is desired to use synchronous inputs, the asynchronous inputs are kept in their inactive state. In addition, both asynchronous inputs are not made active simultaneously [3].

2. Timing Parameters

The most important timing parameters are set-up and hold times, propagation delay, clock pulse HIGH and LOW times, asynchronous input active pulse width, clock transition time and maximum clock frequency [6].The set-up time is the minimum time period for which the synchronous inputs (for example, R, S, J,K and D) and asynchronous inputs (for example, PRESET and CLEAR) must be stable prior to the active clock transition for the flip-flop output to respond reliably at the clock transition. It is usually denoted by t_S (min) and is usually defined separately for synchronous and asynchronous inputs [7].

The hold time t_H(min) is the minimum time period for which the synchronous inputs (R, S, J, K, D must remain stable in the desired logic state after the active clock transition for the flip-flop to respond reliably.Skew Time ($t_{skew\ time}$) - it is the time difference of arrival of two adjacent signal.

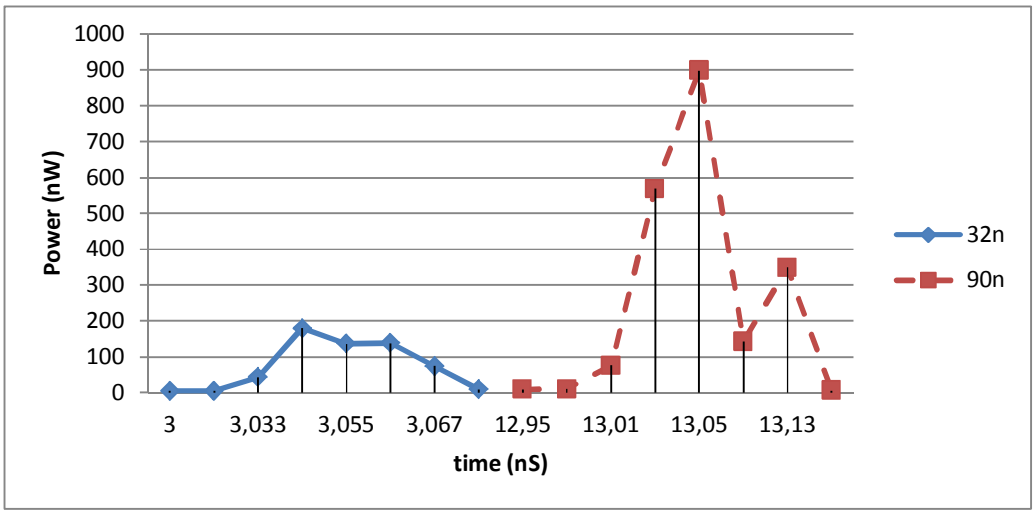


Fig. 4. Comparison of transient rise/fall switching max power response of 32 nm and 90 nm technology.

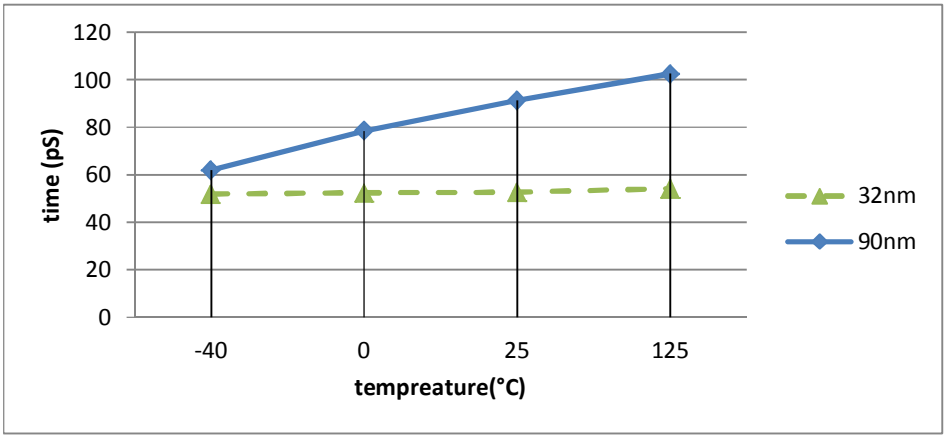


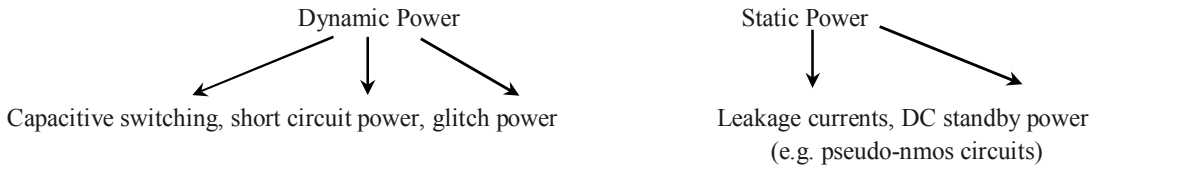
Fig. 5. Comparison of skew depended on temperature of 32nm and 90nm technology.

3. Power Consumption

The power metric used, here is the average power consumed over a constant time interval for various input states and transitions (1).

$$P_{total} = P_{dyn} + P_{static}, (1)$$

$$\bar{P} = f_{ckl} \int_0^{T_{ckl}} Vdd * I_{supply}\, dt. (1.1)$$



Two types of power consumption were measured: the dynamic power and the static power. The Dynamic power is defined as the power consumed by the flip-flop when there is an output transition. The consumption of static power does not depend on transition. Further, static power is state dependent where it is different for different states of the clock, data and output.

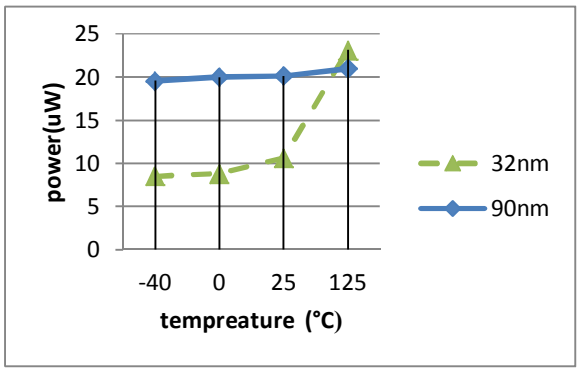


Fig. 6. Comparison of dynamic power depended on temperature of 32nm and 90nm technology.

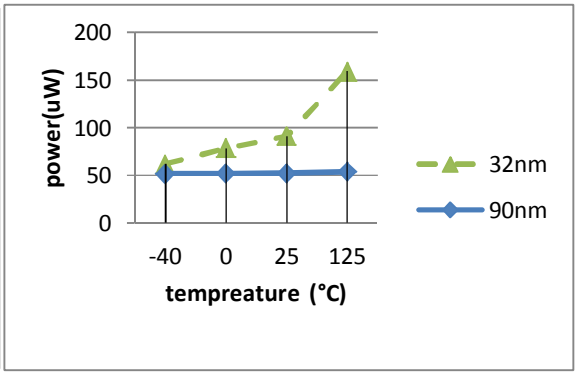


Fig. 7. Comparison of static power depended on temperature of 32 nm and 90nm technology.

For any digital integrated circuit the power can be expressed by following equation (2):

$$P = I_0 + \propto CV^2 ddf\ . \quad (2)$$

Where, I_0 is the leakage current [9], which is governed by the diode equation $I_s\left(e^{qv/kT} - 1\right)$, Vdd is the voltage of power supply, α is the average switching activity factor, C is the total capacitance of the circuit, and f is the operation frequency. The first term in the equation corresponds to the leakage power and the second term corresponds to the dynamic switching power. With the reduction in features sizes, V_{dd} has also decreased, forcing a reduction in the threshold voltage V_t of the transistor. As I_0depends on V_t through diode equation, consequently the leakage current increases [12].

Transition Power

Transition Power is the product of applied voltage to the circuit and current flow through the circuit due to applied voltage source.

$$Power(P)(t) = Voltage(V_{dd}) * Current(I_{dd})(t), \quad (3)$$

Average Power

Static Power Total DC energy was consumed by circuit in unit time.

$$\bar{P} = \frac{E}{T} = \frac{1}{T}\int_0^T (I_{dd}(t) \times V_{dd}(t)), \quad (4)$$

where T is the time, E is the energy in Joule, i_{dd} is the drain current, V_{dd} is the drain voltage.

Conclusions

All measures were done in both technologies. For 90 nm technology, following parameters were taken for typical case: Vdd=1.2 V, Vss=0 input rise and fall time was 50 ps and frequency was 500 MHz.

For 32 nm technology: Vdd=1.05 VVss=0 input rise and fall time was 25 ps 500 MHz.

Temperature for typical case was 25ºC and all parameters were been varied for each corner by (±10%), temperature was changed from -40ºC to 125 ºC.

Measurements of 90nm and 32nm Master Slave Flip-Flop conclude that the skew parameter variation in typical case is approximately 30%.Dinamic power higher in 90nm technology in 25ºC. Static power variation is approximately 50% higher, but in 32nm technology.

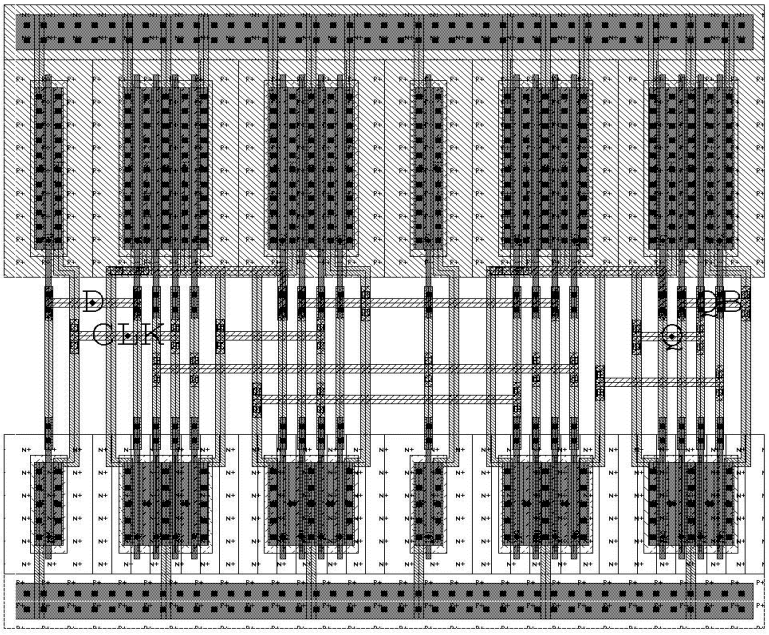


Fig. 8. Layout of CMOS Master Slave Flip-Flop.

Acknowledgements

Design was implemented using SAED 32/28nm and SAED90nm EDK [9] developed by Synopsys Armenia Educational Department. Synopsys tools Design compiler and IC Compiler provided by Synopsys Armenia Educational Department.

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INVENTION OF AN AC/DC CURRENT CONVERTER

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1. Introduction

Currently, powerful LEDs have found widespread applications in various areas, including residential lighting, industry, manufacturing, office and architectural buildings and even street lighting. Such a common use of LEDs is explained by advances in development technology of high-power diodes. It should be mentioned that year by year they confidently displace other, more usual, but outdated sources of domestic and street light (incandescent, halogen, compact fluorescent lamps).

The switching power sources with constant voltage are the major way of LED illumination power source at present [1]. The technique for those is relatively mature and easy to obtain. The current load mainly depends on LED load and the LED brightness is not easy to control, it is the defect for the type of solution to the LED illumination power source. To tackle the defect, LED drivers are used.

Together with powerful LEDs, the electronic market is covered by LEDs drivers providing continuous current for their supply, due to which LEDs uninterrupted operation is ensured and their lifetime is increased. The main function of LEDs drivers is the conversion of AC voltage into direct current (DC). The stabilization of current is carried out by means of linear and pulse converters by different methods [2–4]. An example of LED driver circuit is presented in Fig.1 combining both switching power supply and current adjustment device for the LED converter. The switching power supply is designed in traditional manners. The design points are aimed to stabilize the voltage supply and the electromagnetic interference prevention [1].

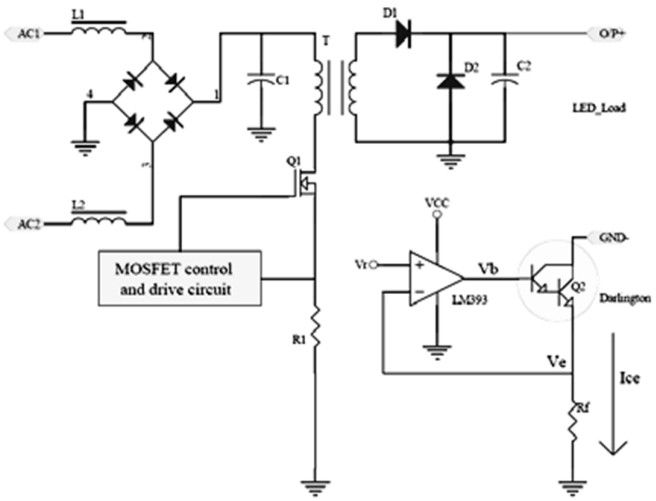

Fig. 1. LED Driver Circuit [4].

There are different circuits of power/voltage converters [1–4]. In this paper, we offer AC/DC voltage converter, which is intended to be used in the future designing of LEDs drivers and other power supply systems. The purpose of the invention is to increase the reliability of the existing converters and to ensure the current stability of the load.

2. Results and Discussion

In Fig. 2 and Fig. 3 the main and the simplified equivalent electrical schemes of the converter, which is described below, are represented, respectively.

The converter has a consecutively connected transistor switches (1,2) and diodes (3,4), between the common points of which a commuting capacitor is connected. The main point of the transistor (2) and the diode (4) is form the positive terminal of the load. The converter has a three-phase uncontrolled bridge consisting of one group of cathode (6) and anode (7) of diodes each, damper capacitor (8), one of the plates of which is connected to negative terminal, and the other plate– to additional diode (9), the cathode of which is connected between the collector of the first transistor switch (1) and the common point of cathode groups of additional diodes (10). The load (11) is connected between positive and negative output terminal. The converter has also inductivities of supply network phases, which are connected via diodes (10) from cathode groups to the capacitor (8).

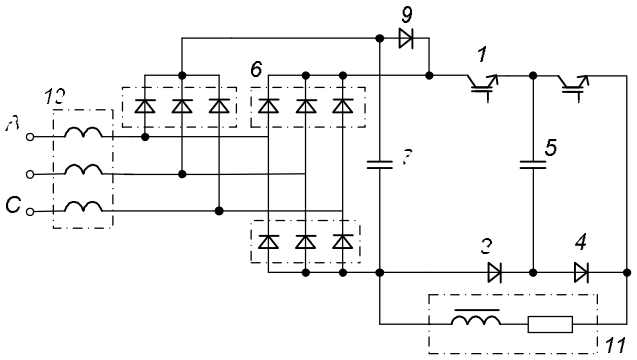

Fig. 2. The electrical scheme of the converter.

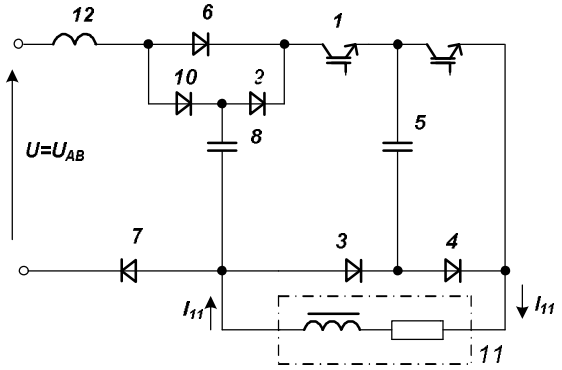

Fig. 3. The equivalent electrical scheme of the converter.

The converter works as follows. To be clear, we assume that the valves are ideal, the load (11) is active inductive and the ratio of the inductivity and the active component is such that the current is uninterrupted by the load. Before t_0 moment all valves are closed and the current of the load (11) is shut off by the diodes. The damper capacitor (8) is charged by $U_{AB} - 12 - 10 - 7$ chain up to $U_{C_8} = U_{\max} \approx U + \rho_8 L_{12}$, where U is the linear voltage, U_{C_8} is the voltage of the capacitor (8), $\rho_8 = \sqrt{L_{12}/C_8}$ is the wave resistance (L_{12} is the inductivity of the network supply, C_8 is the capacity of the capacitor (8)). At time t_0 a control impulse is given to the transistor (1), which is opening and the capacitor (5) is charged via the following chain: the positive plate of the capacitor–transistor (1)– capacitor (5)–diode (4) – load (11)– the negative plate of the capacitor. At time t_1 the voltage on the capacitors is equal to the voltage U (the linear voltage of the chain), beginning from t_1 the diodes (6,7,9) are opened and the capacitors (5,8) are charged simultaneously up to $U_{C_5} = U_{C_8} = U_{\max}$, where U_{C_5} is the voltage of the capacitor (5).

In time diagrams the dynamics of mutual offs of diodes and separate elements are shown in Fig. 4. At time t_2 an opening impulse is given to transistor (2) and a closing impulse to transistor (1), due to which the capacitor (8) continues to be charged via diodes (7,10) up to $U_{\max}$, and the capacitor (5) is discharged via the load circuit according to the following chain: the upper plate of the capacitor (5) – transistor (2) – load (11) – diode (3) – the lower plate of the capacitor (5).

At time t_3 the commuting capacitor is discharged to zero voltage and at t_3 moment the current of the load (11) is closed via oppositely connected diodes (3,4). Beginning from t_4 moment the electromagnetic processes in scheme are repeated.

As it could be seen from the time diagrams explaining the scheme, hyper voltages cannot exceed the voltage on the damper capacitor and it is possible to limit the hyper voltages up to a sufficient level by choosing the corresponding capacity of the capacitor (8).

3. Conclusion

There is no necessity for the control algorithms to oversee the hyper voltages. In the suggested scheme, it is implemented automatically since in order to oversee the hyper voltages naturally commuting uncontrolled elements– diodes, are used. It significantly increases the reliability of the scheme performing simple control algorithm simultaneously. Only two controlled switches (1,2) are used in the scheme, which work in antiphase frequency - pulse control regime, due to which the

load current stability is ensured. Modern IGBT transistors are chosen as controlled valves, due to which it is possible to significantly increase the operating frequency of the scheme, thence, reducing the proportions of the smoothing output throttle, ensuring the current sufficient smoothing. It leads to increase the reliability of the converter performing relatively simpler control algorithms.

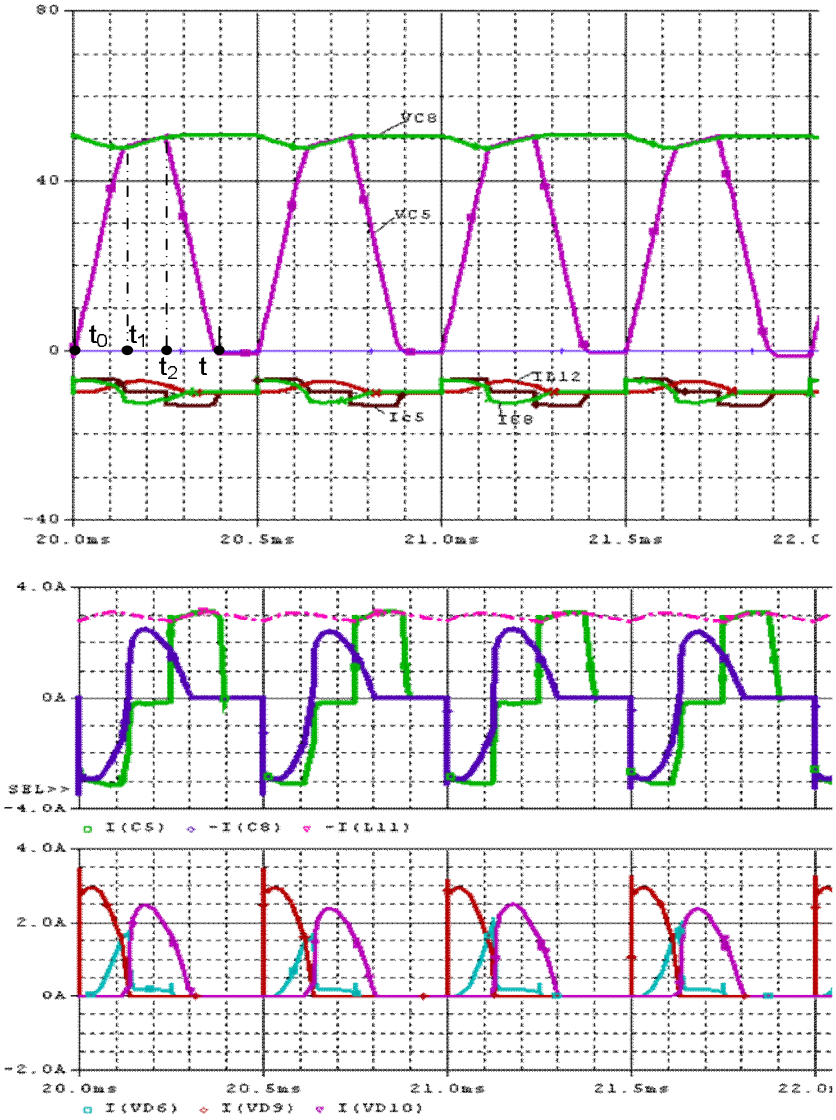

Fig. 4. Time diagrams explaining the invention.

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CMOS PID CONTROLLER FOR TEMPERATURE CONTROL SYSTEM

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1. Introduction

One of the most important and challenging areas for research in technological installations for production of thesemiconductor devices is temperature control. The modern control systems use PID (proportional integral derivative) controllers.
This article presents a new approach to implement PID controller by using new technologies. The proposed architecture provides more flexibility. The suggested design is based on CMOS transistors. The presented mechanism of PID controller can be used in different control systems, such as temperature control system, power control system etc. Different configurations for PID controller are implemented and compared with each other.
The PID controller is one of the most common control algorithms. The most practical feedback loops are based on PID control or some minor variations of it [1]. PID controllers are widely used in process control industry due to relatively simple structure and easiness in implementation [2-4].
The principle structure of PID controller is presented in Fig. 1.

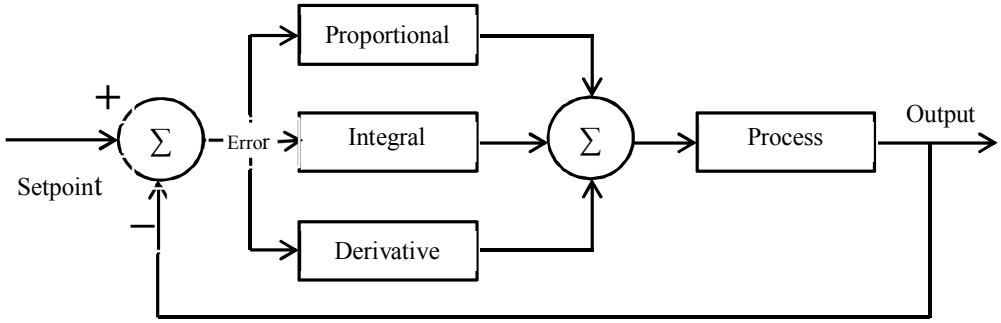


Fig. 1. PID Controller principle structure.

PID controller can be implementedwith theanalog circuits or with thesoftware (using microcontrollers).
Both methods have advantages and disadvantages:

- Analog PID controllers are common in many applications. They can be easily constructed using analog devices such as operational amplifiers, capacitors and resistors. They are reliable in mechanical feedback systems, and able to satisfy many control problems. The advantage of this method is continuous operation, and the disadvantage of this method is that, it is difficult to tune the constant.
- Software implementation's method advantage is that with this method the controller parameters can be tuned and adjusted easily. So, this property makes it flexible, but has the disadvantages:it is not continuous and the microcontroller resources are mostly used for PID algorithm than for other activities. Digital PID controllers eliminate ADC and DAC conversion and the associated problems, such as delay. So, analog implementation is faster than digital implementation.

So, based on the requirements of the problem we can choose which method to use.

2. CMOS PID Controller

The textbook equation of the PID controller is

$$u(t) = k_p e(t) + k_i \int_0^t e(\tau)d\tau + k_d \frac{d}{dt} e(t), \quad (1)$$

where u is the control signal and e is the control error. The control signal is thus a sum of three terms: the P-term (which is proportional to the error), the I-term (which is proportional to the integral of the error), and the D-term (which is proportional to the derivative of the error). The controller parameters are proportional gain k_p, integral gain k_i and derivative gain k_d. The controller can also be parameterized as

$$u(t) = k\left(e(t) + \frac{1}{T_i}\int_0^t e(\tau)d\tau + T_d \frac{de(t)}{dt}\right), \quad (2)$$

where T_i is called integral time and T_d derivative time [1-4].

$$k_p = k,$$
$$k_i = k\frac{1}{T_i}, \tag{3}$$
$$k_d = kT_d.$$

Below are presented P, PI, PD and PID controllers' models with their response characteristics, based on the resistors and the CMOS transistors. In models we are using operational amplifier, which is real op-amp, and designed by us.

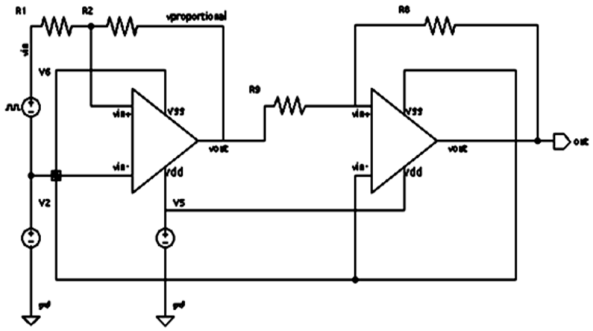
P (proportional) controller

The equation of P controller is:

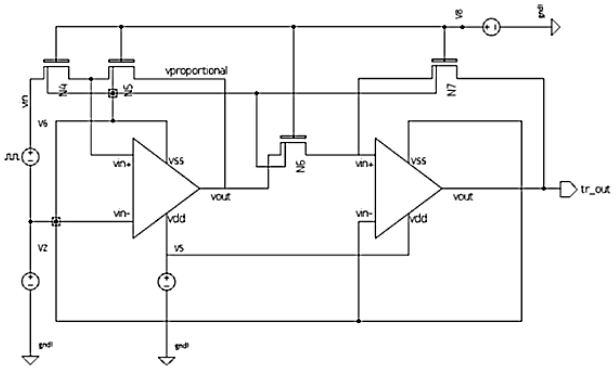
$$u(t) = k_p e(t). \tag{4}$$

Proportional control is the most basic control that is always used in the controllers. It's easy to develop, but it's not able to remove the steady-state error.

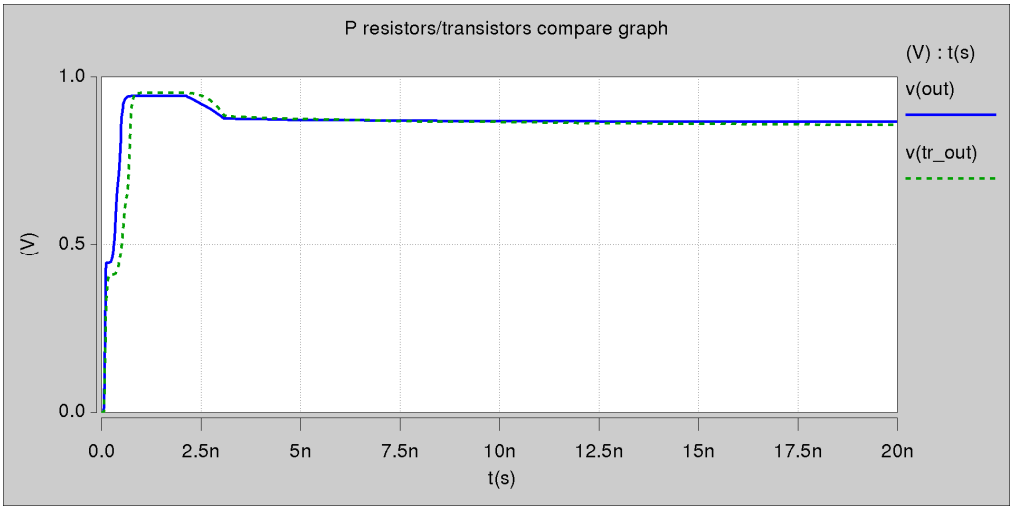
In Fig. 2a and in Fig. 2b P controllers' models based on resistors and CMOS transistors respectively are presented, and in the Fig. 2 the comparison of their response characteristics is presented.



a) Controller's model with resistors.



b) P controller's model with CMOS transistors.



c) Comparison result of the response characteristics of P controllers with resistors (v(out)) and CMOS transistors (v(tr_out)).

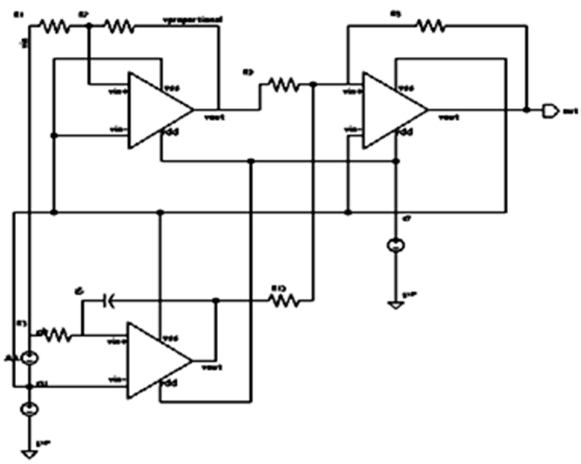
Fig. 2. P controller.

PI (proportional-integral) controller

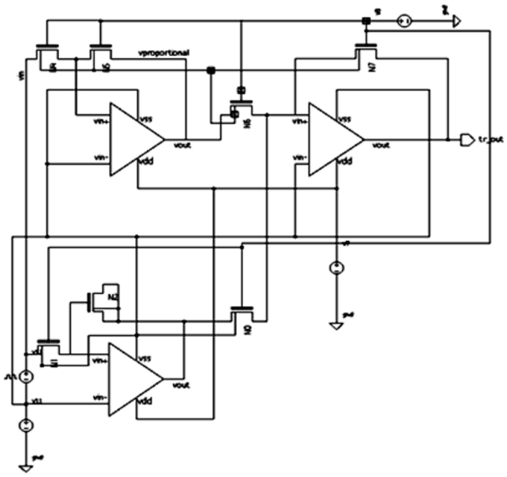
The equation of PI controller is:

$$u(t) = k_p e(t) + k_i \int_0^t e(\tau)d\tau. \tag{5}$$

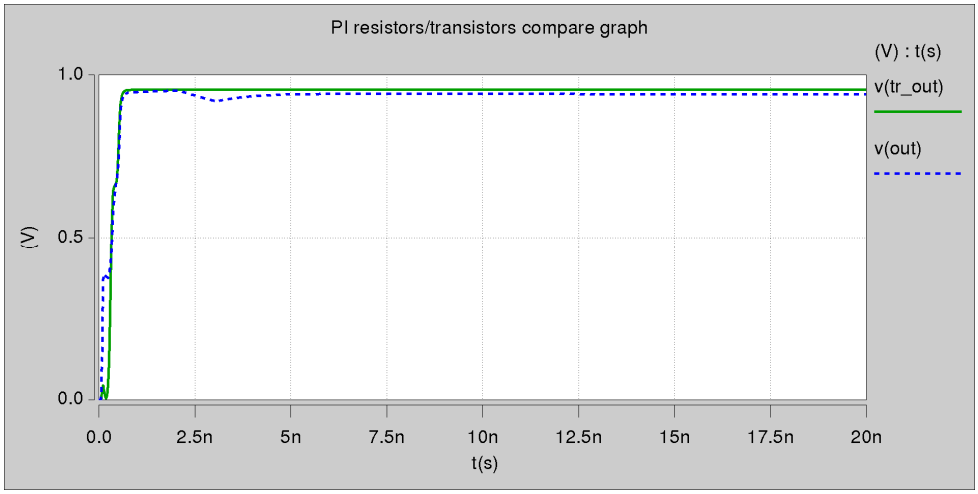
Proportional-Integral controller is used to eliminate steady-state error, but if integral gain is mistuned, the system can become unstable and the response time can be slower.
In Fig. 3a and Fig. 3b PI controllers' models based on resistors and CMOS transistors respectively are presented, and in the Fig. 3.cthe comparison of their response characteristicsis presented.



a) PI controller's model with resistors.



b) PI controller's model with CMOS transistors.



c) Comparison result of the response characteristics of PI controllers with resistors (v(out)) and CMOS transistors (v(tr_out)).

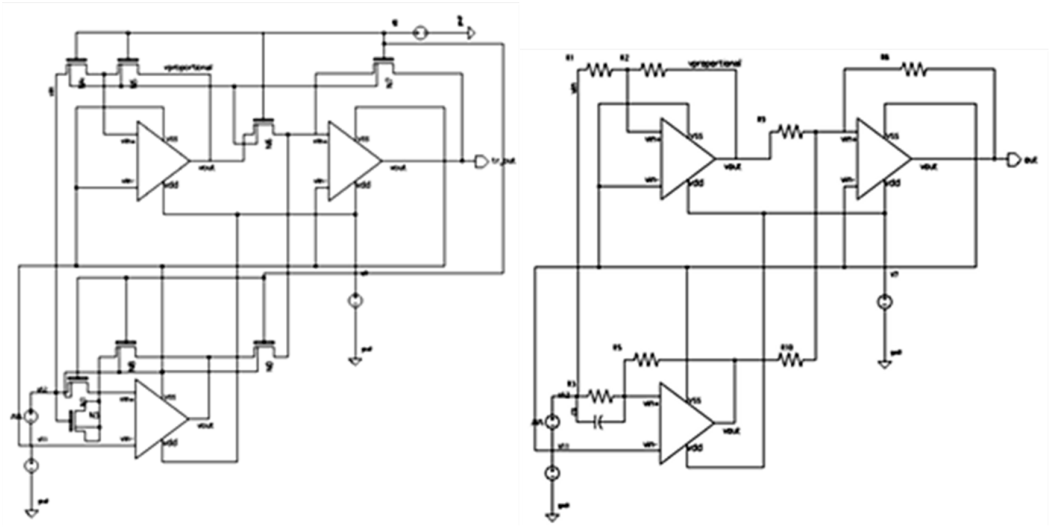
Fig. 3. PI controller.

PD (proportional-derivative) controller

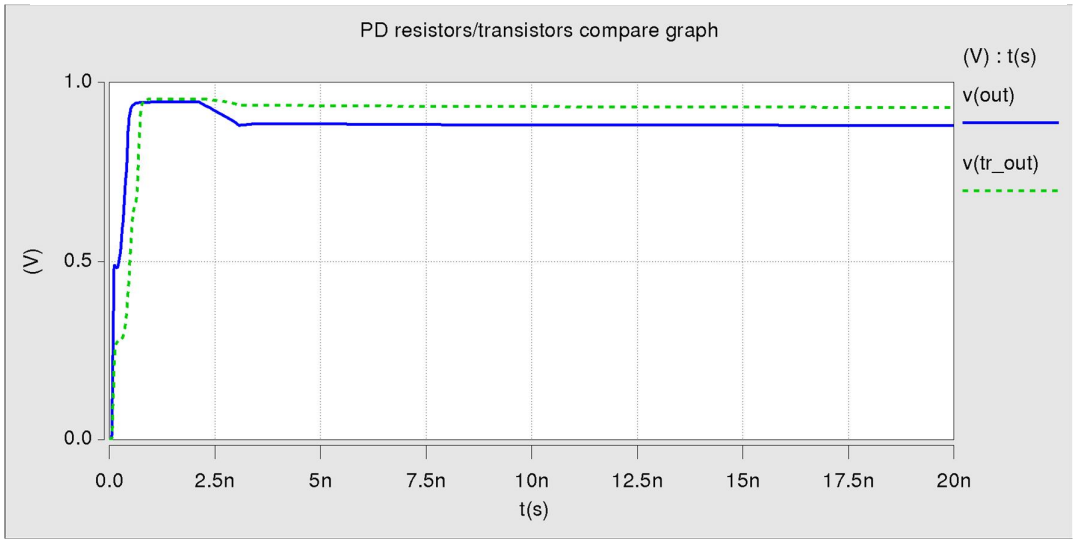
The equation of PD controller is:

$$u(t) = k_p e(t) + k_d \frac{d}{dt} e(t). \quad (6)$$

PD control increases the stability of the system and makes the response time faster, but with the presence of the noise in the system, it can increase the differential portion of the equation resulting in a negative effect for the input.
In Fig. 4.a and in Fig. 4.b PD controllers' models based on resistors and CMOS transistors respectively are presented, and in the Fig. 4.c the comparison of their response characteristics is presented.



a) PD controller's model with resistors. b) PD controller's model with CMOS transistors



c) Comparison result of the response characteristics of PD controllers with resistors (v(out)) and CMOS transistors(v(tr_out)).

Fig. 4. PD controller.

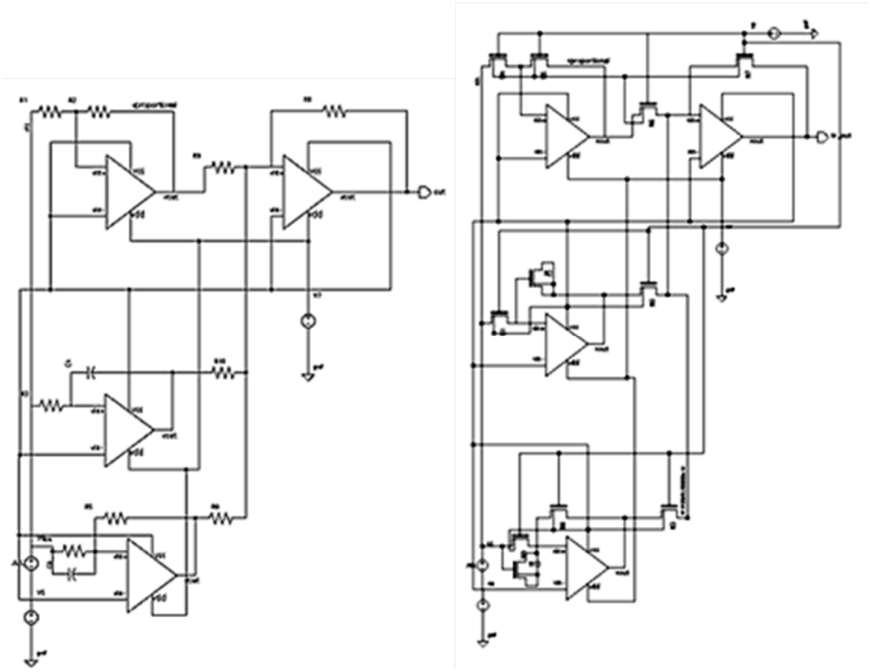
PID (proportional-integral-derivative) controller

Actual control of the PID controller is the combination of P, I and D controls.

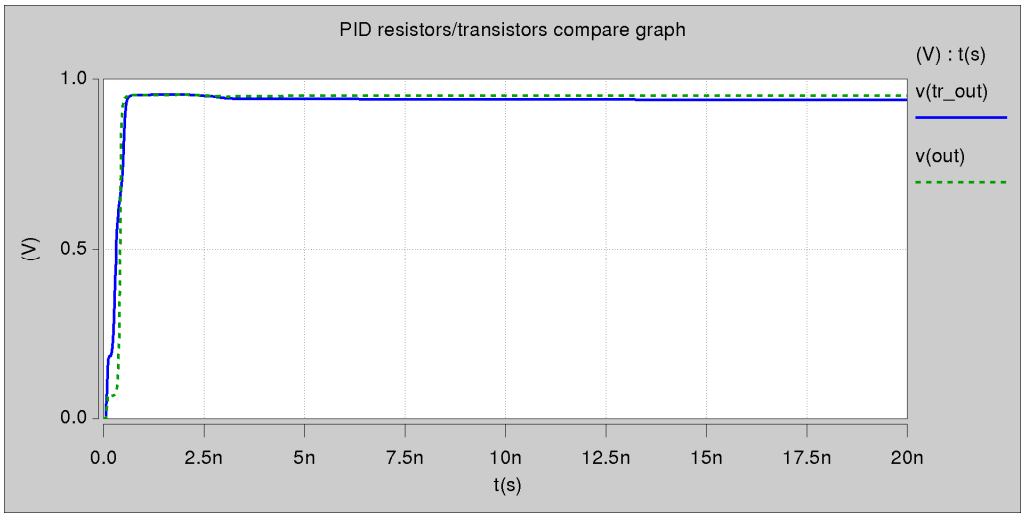
In Fig. 5.a and in Fig. 5.b PID controllers' models based on resistors and CMOS transistors respectivelyare presented, and in the Fig. 5.cthe comparison of their response characteristics is presented.

3. Conclusion

We have presented comparative analysis for P, PI, PD, PID controllers with resistors and CMOS transistors. As we can see from comparative response characteristics, we get similar result for all the controllers. So, we suggest using CMOS transistors instead of resistors, because they will make P, PI, PD, PID controller's gains more flexible. We can make resistors from cascade of CMOS transistors, and we can connect the gates of transistors to output of decoder. In this way we can easily change controllers' gains (k_p, k_i, k_d). By giving different combinations to decoder inputs, we can switch on and switch off transistors, so the resistance of transistors will be changed, which will cause the change of controllers' gains. So, the proposed method allows designing flexible PID controller without any software implementation.



a) PID controller's model with resitors. b) PID controller's model with CMOS transistors.



c) Comparison result of the response characteristics of PID controllers with resistors (v(out)) and CMOS transistors (v(tr_out))/

Fig. 5. PID controller/

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CONTENTS

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